Bulletin of Electrical Engineering and Informatics
ISSN: 2302-9285
Vol. 6, No. 2, June 2017, pp. 122~132, DOI: 10.11591/eei.v6i2.597

Stack Contention-alleviated Precharge Keeper for Pseudo Domino Logic

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Abstract

The dynamic circuits are supposed to offer superior speed and low power dissipation over static CMOS circuits. The domino logic circuits are used for high system performance but suffer from the precharge pulse degradation. This article provides different design topologies on the domino circuits to overcome the charge sharing and charge leakage with reference to the power dissipation and delay. The precharge keeper circuit has been proposed such that the keeper transistors also work as the precharge transistors to realize multiple output function. The performance improvement of the circuit's analysis have been done for adders and logic gates using HSPICE tool. The proposed keeper techniques reveal lower power dissipation and lesser delay over the standard keeper circuit with less transistor count for different process variation.

Keywords*: power consumption, domino logic, keeper circuit, charge sharing, stack effect*

1. Introduction

Dynamic logic designs offer a lot of remarkable features such as low transistors count (almost half as compared to static design), reduced load capacitance and improved speed [1-2] and it is preferred as compared to static logic design. A large number of applications including memory, high performance microprocessor and high speed digital circuits take advantage of these designs.

The pseudo domino buffer [2] improves the cascading capability as well as the charge sharing problem but offer more delay and power consumption. These disadvantages have been taken care by varying the body bias using multiple power supply [3-4]. The several keeper circuit use for multiple output functions along with many precharge transistors in single domino circuit [4]. The reverse and forward body bias techniques are also applied on keeper for better performance on account of extra supply. A feedback keeper overcomes the charge sharing problem but its operation conflicts with speed and power [5] and it solution is to regulate the voltage without any size optimization at the cost of low swing [6].

The tuning of the voltage feedback circuit using a transistor and another power supply improves the performance [6]. The nMOS cascading effect improves the load capacitance in Pull-up Network (PUN) resulting in low swing [7]. The leakage of the evaluation path of deep submicron devices is improved by using stack [8] and the input vector control [9-10] at the cost of area and power.

Improved existing standard keeper technique of pseudo domino circuits produces lower swing and the charge sharing problem at output node during the evaluation phase. The proposed article on keeper techniques overcome the above stated problem of the standard keeper technique in addition to less transistor count, low power dissipation and high speed.

A novel precharge keeper technique has been offered in this article with the aim to use the some keeper transistor as a precharge transistor for several complex functions in the one domino circuit with optimum area. Using the precharge keeper in the pseudo domino circuit can effectively improve the performance while simultaneously resolving the charge sharing problem. The proposed Contention Alleviated Precharge Keeper (CAPK) and proposed Stack Contention Alleviated Precharge Keeper (SCAPK) techniques are also proposed here to alleviate the contention current resulting improvement in the speed and leakage power respectively.

Received March 1, 2017; Revised May 2, 2017; Accepted May 16, 2017

Simulation results validate the proposed design on adders and logic gates and illustrate the power saving and delay minimization as compared to the standard keeper design.

2. Pseudo Domino Circuit

The operation of the single stage dynamic circuit is quite easy over the multistage dynamic design, where the output of the cascaded dynamic circuit is charged to high logic in the precharge phase (CLK=0). In the evaluation phase (CLK=1), the output of the first dynamic circuit discharges fully but the output of the second dynamic circuit discharges to $V_{O1}<V_t$. So the circuit causes a problem to make a transition from high to low during the evaluation phase and an inverter in between the two quell this limitation [1]. This circuit is referred as domino logic. The inclusion of an inverter facilitates the discharging path for the output of the second dynamic stage in the evaluation phase. However, the major difficulty of the dynamic logic is that it is more sensitive to noise and dissipates unwanted power during the precharge phase.

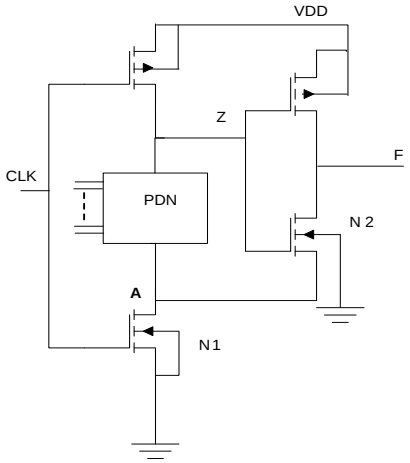

Figure 1. Pseudo domino circuit

The performance degradation due to the propagation of the precharge phase condition of the domino logic circuits can be improved using the pseudo domino circuit as in Figure 1. The source terminal of the transistor N2 of the static CMOS inverter connects to the drain terminal of the evaluation transistor N1 at node A, instead of ground [2]. Therefore, the value of the dynamic output node Z cannot propagate to the domino output node F during the precharge phase as the evaluation transistor N1 remains in OFF state.

This configuration saves power up to 18% as compared to the conventional domino logic design. This topology is essential for the performance improvement of the domino logic circuit in the precharge phase and also applicable for the pull up network in the P-type domino logic design [2]. However, the pseudo domino logic circuit due to short circuit paths suffers from the charge sharing and the charge leakage problem.

3. Charge Sharing Problem

The voltage of the output node F in the pseudo domino circuit becomes lower due to the charge sharing problem. When all the inputs of the pull-down network are set to '1' in the precharge phase, the voltage drops at the output node Z for the path shown in Figure 2.

This voltage drop could be propagated to the next node F. The output voltage at node F shares the charge from capacitor C1 to C2 as N2 transistor is ON. Consequently, the performance of the pseudo domino circuit due to the voltage drop at output node F is degraded in terms of the speed and the power dissipation. The voltage drop can be reduced by reducing the intermediate node capacitance of PDN network [2].

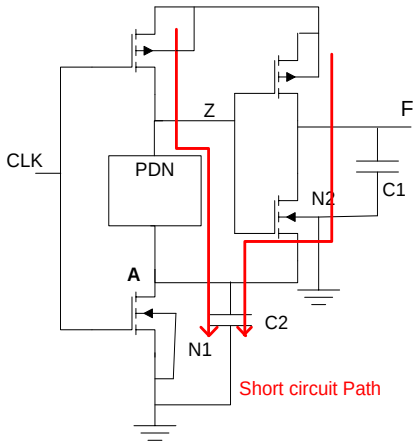

Figure 2. Charge sharing problem in pseudo domino circuit

If the value of the load capacitor C1 is equal to the capacitance C2, then the output node voltage becomes VDD/2. The simplest solution to this is to make load capacitor much larger than the other charge sharing capacitors (C2) and the other solution is to use the keeper circuit [1].

In conventional domino design, 50% of the clock cycle is used for the evaluation phase and the output voltage will be reset to low logic during the precharge phase. For the pseudo domino logic circuits, evaluated output results are held during the precharge phase in cascading [2]. For upcoming stages, the output value can be generated in the precharge phase by enabling PDN transistors and N2. This feature supports the result for a long cascade of the pseudo domino logic to be settled even during the precharge phase. The different keeper techniques have been used on the pseudo domino circuits for the performance improvement in this article.

4. Keeper Circuit Topologies

A few of the keeper designs have been considered to solve the charge sharing problem to keep the output at correct level. The keeper transistor should be sufficiently strong in terms of size to overcome the leakage current.

4.1. Pseudo Domino Logic Using Standard Keeper Circuit

An extra transistor P_{SK} along with an inverter at the output node F in the domino circuit is called standard keeper circuit as in Figure 3. The transistor P_{SK} conducts only when the output node F of the domino logic goes high. Thus, the output node F of the domino circuit does not show any voltage drop on the precharge phase at the cost of increased power delay product because of the extra transistors [2-3]. The output of the standard keeper configuration provides low swing and always remains at logic 1 as illustrated in Figure 4 during the evaluation phase.

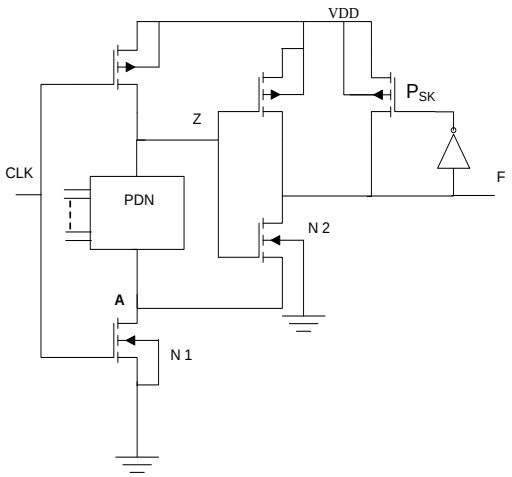

Figure 3. Pseudo domino logic using standard keeper circuit

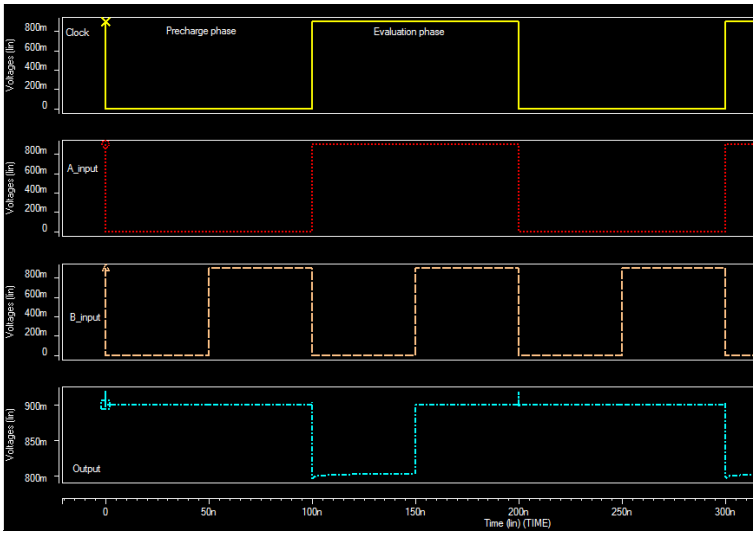

Figure 4. Charge sharing and /or charge leakage problem of 2-Input AND gate using standard keeper technique

Reduction in the supply voltage of the standard keeper circuit diminish the power dissipation of the pseudo domino logic without conflict the circuit operation. The self-biased pMOS as a diode can cascade with the P_{SK} pMOS in the standard keeper circuit to increase the stand by current without any optimization [4-7]. The self-biased standard keeper circuit is not suitable for the high speed operation as the voltage drop occurs at the output node in the precharge phase. Therefore this technique is not preferred.

4.2. Pseudo Domino Logic Using Precharge Keeper Circuit

A further solution to the charge sharing problem is enhanced by the addition of the clock driven keeper transistor P_{PK} as in Figure 5. The precharging of the internal node becomes effective to eliminate the charge sharing problem in evaluation phase as shown in Figure 6. In the evaluation phase, the precharge keeper transistor P_{PK} is turned on and the dynamic node F is charged fully to VDD according to the input values as depicted in Figure 6. The precharge keeper technique resolves the charge sharing problem of the standard keeper circuit [12].

Not only the precharge keeper circuit is used to reduce the charge sharing and the charge leakage, but also several complex logic functions can be realized with less number of

transistors in single dynamic design. In previous design, multiple keeper had been used to design the multiple functions with multi precharge transistor [4]. The precharge keeper is used as a precharge transistor for multiple output function along with the keeper circuit. Consequently the precharge keeper circuit is ismore efficient in terms of the static and dynamic power and the delay for the pseudo domino design.

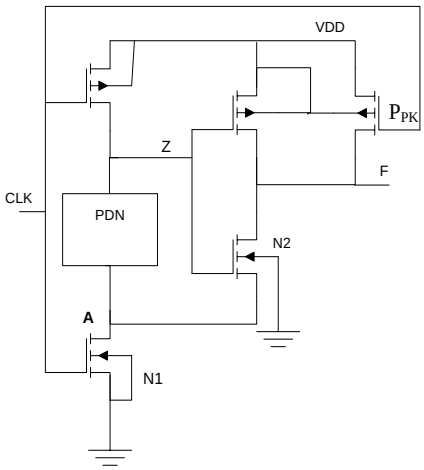

Figure 5. Pseudo domino logic circuit using proposed precharge keeper circuit

The speed and power of the precharge keeper technique can be improved using the variable threshold keeper [3] or dual threshold voltage [11] in the pseudo domino circuits. In the variable threshold keeper, the bulk terminal of the precharge keeper transistor P_{PK} is connected to another power supply of higher value to apply the reverse substrate bias voltage. Thus the current obtained by the high threshold voltage keeper is reduced that does not degrade the noise immunity and improves the power consumption at the cost of multiple power supply.

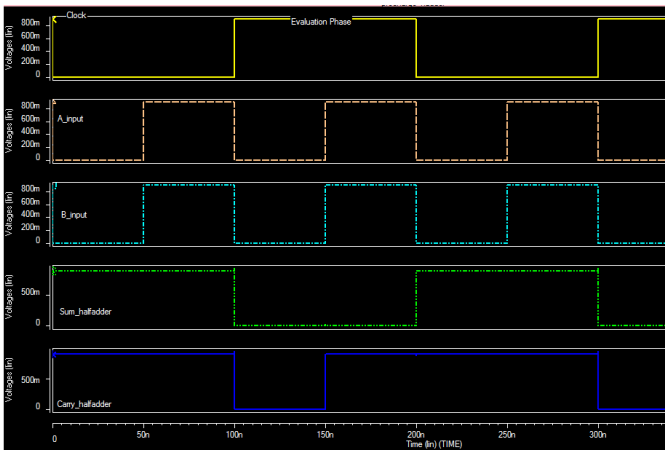

Figure 6. Simulation result of half adder using proposed precharge keeper circuit at 32 nm technology

4.3. Pseudo Domino Logic Using Proposed Contention-alleviated Precharge Keeper (CAPK)

The proposed precharge keeper technique has been modified here to alleviate the problem of the contention current by reducing the gate voltage of the precharge keeper

transistor P_{PK} instead of reducing its effective supply voltage which increases the threshold voltage drop. A pass transistor is inserted in between the gate terminal of the precharge keeper transistor P_{PK} and the clock signal CLK as well as shorting the gate of the pass transistor to ground.

The source potential of the pass transistor is low at the precharge phase, so the voltage of node Y will be the absolute value of the threshold voltage of the pass transistor. The gate voltage of the precharge keeper P_{PK} is reduced by the threshold voltage of the pass transistor ($|V_{tp}|$) instead of reducing the supply voltage when source terminal of pass transistor is connected with GND.

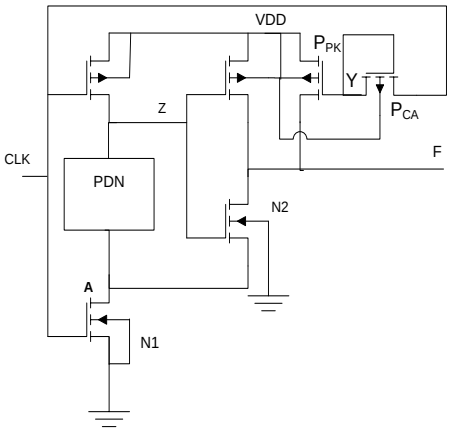

Figure 7. Proposed Contention-Alleviated Precharge Keeper circuit (CAPK) with pseudo domino logic

The contention-alleviated precharge keeper (CAPK) circuit is proposed here with one self-biased pass transistor P_{CA} as displayed in Figure 7. The gate potential of pMOS (P_{PK}) is reduced as compared to previous proposed design. Therefore the precharge keeper transistor P_{PK} is still active with low current. The contention-alleviated precharge keeper circuit has been demonstrated to enhance the speed and power of the pseudo domino circuit with less transistor count as compare to the standard keeper technique.

The contention-alleviated precharge keeper circuit can be enhanced by applying the higher potential between V_{GS} of the pass transistor. The gate potential of the precharge keeper transistor is confined between VDD to $V_{bias}+|V_{tp}|$ so the pull-up strength of the precharge keeper transistor P_{PK} can be suitably reduced for high supply voltage. This will help to vary the biasing of the pass transistor P_{CA} that reduce the power consumption. The effectiveness of the contention-alleviated precharge keeper technique is little improved as the supply voltage is elevated till P_{CA} remains ON. The improvement referred concern better power delay product at the cost of additional power supply. Thus CAPK is better design configuration as modified CAPK and other discussed design.

4.4. Pseudo Domino Logic Using Stack Contention-alleviated Precharge Keeper (SCAPK)

The leakage current in the deep-submicron devices results from the subthreshold and the gate leakage as the technology scales down. The subthreshold leakage current depends on the threshold voltage V_t and the controlling voltages (V_{GS} & V_{DS}). The first solution to the problem is the technology based that uses higher V_t with thicker gate oxide t_{ox} to support the reduction in the leakage current. The other solution is based on the circuit that stacks the cells [8-10].

The aim of the stack is to minimize the controlling voltage and increase the bulk potential of the stack transistors resulting in the reduction of the subthreshold current and increment of the threshold voltage respectively. The leakage of the transistors in the stack is a function of the number of transistors and the input patterns.

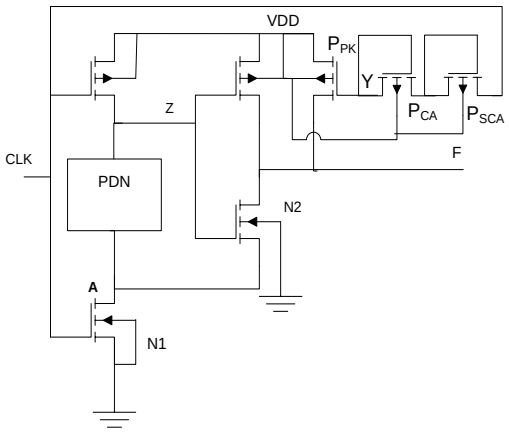

Figure 8. Proposed Stack Contention Alleviated Precharge Keeper (SCAPK) with pseudo domino logic

The leakage current of the domino logic in Figure 8 is reduced by connecting one extra transistor P_{SCA} in contention-alleviated precharge keeper circuit as the stack. The source potential of the stack transistor P_{SCA} will be a slightly lower than the source potential of the alleviated transistor P_{CA} in the stack. Therefor the controlling voltage V_{DS} and the bulk potential of the stack transistor P_{SCA} will be higher as compare to the alleviated transistor P_{CA} resulting into increment of the threshold voltage to reduce the leakage current. Thus the pull-up strength of the P_{PK} can be reduced for high supply voltage. The proposed stack contention-alleviated precharge keeper (SCAPK) pseudo domino circuit yields better operating speed and low leakage current than the standard keeper circuit.

5. Results and Discussion

The aim of this article is to design an improved pseudo domino circuit by applying suitable keeper configurations. The precharge pulse in the conventional domino logic design is transmitted to the output stage that increases the power loss significantly and limits the cascading performance of the gate. So the pseudo domino design is used to improve the precharge pulse degradation. However the charge sharing problem of the pseudo domino circuit is solved by introducing the keeper circuits that supplies a limited amount of the current at the output node. However, the standard keeper circuit having more transistor count dissipate higher power. So the precharge keeper circuit has been designed with one transistor that is forced to become ON in the precharge condition only.

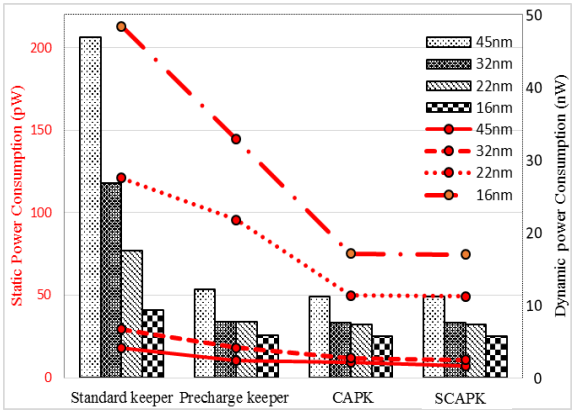

Figure 9. Two input AND gate simulation result for static and dynamic power consumption

The precharging of the keeper circuit is useful to minimize the power loss and the transistor count. Additionally the precharge keeper transistor is used to charge the intermediate nodes of the domino circuits to solve the charge sharing problem therefore the several output function can be designed in one pseudo domino logic.

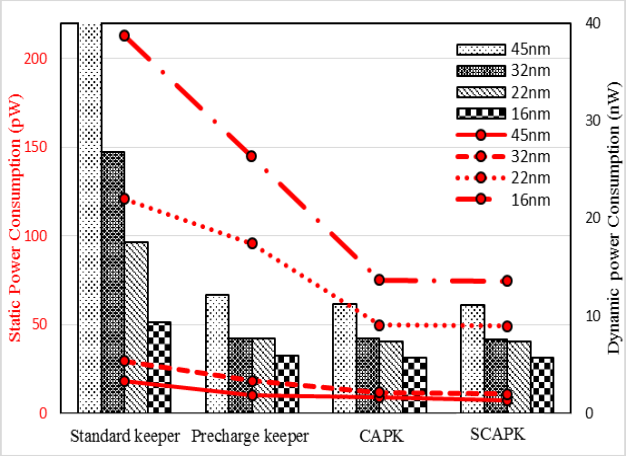

Figure 10. Two input OR gate simulation result for static and dynamic power consumption

The contention alleviated precharge keeper has been designed to reduce the contention current and improve the operating speed. The static power consumption of the pseudo domino circuit can be reduced by stack.

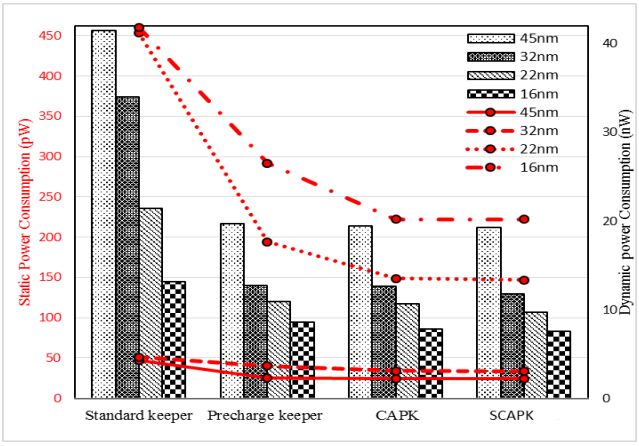

Figure 11. XOR gate simulation result for static and dynamic power consumption for design configurations

The different design techniques of the pseudo domino circuit in Figure 9. show the graphical representation of the two input AND gate for the power dissipation. In all simulation results, line and bar graph plots depict the static and dynamic power consumption, respectively, for different design configurations. Simulation results are summarized in Figures 9-15 illustrate that the static as well as dynamic power dissipation have been reduced for different proposed keeper designs such as logic gates, adders etc. and compared to the standard keeper pseudo domino circuit.

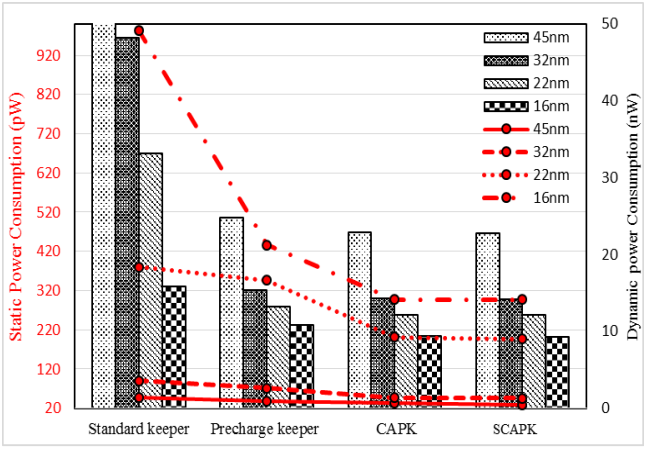

Figure 12. Half adder simulation result for static and dynamic power consumption

Figure 13 revels that the proposed precharge keeper for 1-bit full adder circuit reduces the both static and dynamic power dissipation by 60% and 28% respectively as compared to the previous designed standard keeper techniques. Thus the precharge keeper pseudo domino circuit has been designed to improve the power dissipation with minimal transistor count that provide dual function of precharge transistor and keeper transistor. From Figure 14, it is clear that proposed techniques have lower static and dynamic power consumption for 8-bit full adder.

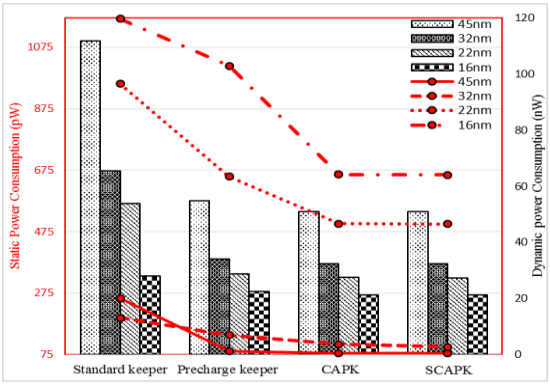

Figure 13. 1-bit Full adder simulation result for static and dynamic power consumption

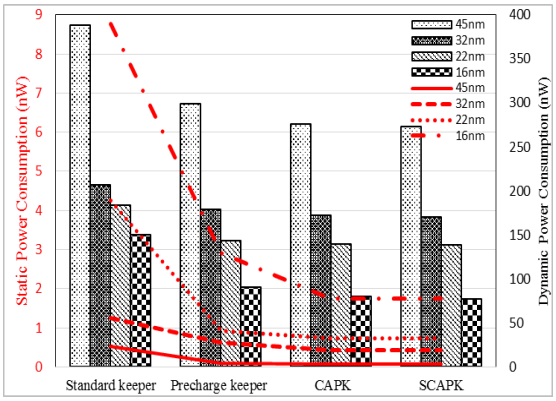

Figure 14. 8-bit Full adder simulation result for static and dynamic power consumption

The comparative analysis of various proposed keeper circuits are demonstrated in terms of the delay for different design configuration as depicted in Table 1. The output of the standard keeper circuit always stay on high logic for all digital circuits. These disadvantages have been resolved by proposed designs. The delay and the leakage improvement in the proposed SCAPK technique for 1-bit full-adder ranges up to 60% and 15% respectively with respect to the proposed precharge keeper circuit.

Thus the circuit performance has been enhanced for mentioned digital circuits as compare to previous designed techniques. As observed from the Table 1, the proposed SCAPK circuit reduces the delay as compared to the proposed precharge keeper technique discussed in the article.

Table 1. Delay Minimization (ps) of Proposed Keeper Circuits for Different Process Variation

Technology	Proposed Keeper circuits	AND gate (ps)	OR gate (ps)	XOR gate (ps)	Half adder (ps)	1-Bit Full adder (ps)	8-Bit Full adder (ps)
45nm	Precharge keeper	54	54	95	70	69	91
	CAPK	44	44	94	61	62	89
	SCAPK	43	43	94	42	62	88
32nm	Precharge keeper	62	62	108	78	80	99
	CAPK	53	53	107	50	73	97
	SCAPK	53	52	106	48	71	97
22nm	Precharge keeper	80	80	134	111	122	134
	CAPK	72	72	133	72	96	133
	SCAPK	71	71	132	72	95	132
16nm	Precharge keeper	107	107	173	165	204	224
	CAPK	96	96	170	83	192	215
	SCAPK	96	96	167	82	191	208

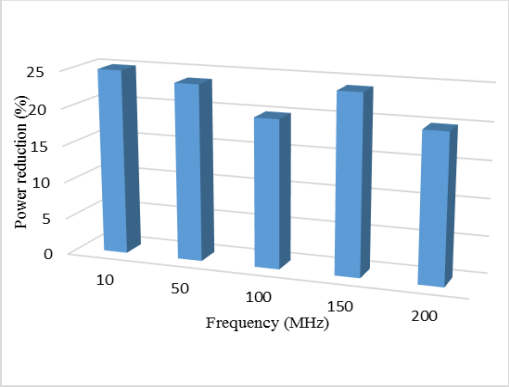

Figure 15. Power reduction (%) of the proposed SCAPK technique and exciting standard keeper technique for different frequencies

Power reduction (%) of the proposed SCAPK technique and exciting standard keeper technique is shown in Figure 15 for different frequencies. It is clear that the SCAPK technique reduces the power consumption.

5. Conclusion

The proposed design techniques are more effective in reducing the charge sharing problem of the pseudo domino logic circuit which eliminates the precharge pulse degradation in the domino logic. Existing and proposed circuits have been simulated with HSPICE tool at different design technology such as 45nm, 32nm, 22nm and 16nm. The pseudo domino circuit

with precharge keeper reduces the power and delay considerably along with only one transistor as a keeper circuit.

All proposed keeper techniques have been compared with the standard keeper technique in terms of power reduction. It becomes evident from Figures 9-14 that the proposed SCAPK pseudo domino circuit at 16nm technology reduces the total power consumption up to 57% , 54%, 57% in XOR gate, half-adder and 1-bit full adder circuit respectively. Proposed SCAPK circuit has improved delay, static and dynamic power dissipation as compared to other topologies. Therefore, proposed keeper circuits are superior design, especially for adder, those are widely used in many VLSI systems such as microprocessors, arithmetic logic unit (ALU), Multiplexer, DSP architecture and code converter so here adders and logic gates has been improved in terms of power and speed.

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