Bulletin of Electrical Engineering and Informatics
Vol. 4, No. 3, September 2015, pp. 186~195
ISSN: 2089-3191

Reduction of switches and DC sources in Cascaded Multilevel Inverter

N. Devarajan, A. Reena*
Department of Electrical and Electronics Engineering
Government College of Technology, Coimbatore -641 013
*Corresonding author, email: reenalightening@gmail.com

Abstract

This paper presents a new proposed cascaded multilevel inverter module of low cost and high efficiency which is being a demand in the industrial drive applications. The presence of harmonics and increasing number of switches and DC sources for higher level is the major issue in the usage of cascaded multilevel inverter for the application of medium and high voltage power systems. In this proposed work several new techniques were introduced to reduce the number of switches and DC sources, which overcome the disadvantages of cascaded multilevel inverter. The THD values for various levels (seven& nine) are compared by simulating the proposed module in the MATLAB environment, with and without using soft switching techniques like PWM, SPWM and the reduction of THDs and compactness of the proposed module are validated.

Keywords*: Harmonics, Cascaded Multilevel Inverter (CMLI), Pulse Width Modulation (PWM), Sinusoidal Pulse Width Modulation (SPWM), Total Harmonic Distortion (THD), Flexible AC Transmission Systems (FACTS)*

1. Introduction

Recent advancement of medium and high voltage power system applications like Static Var Compensator (SVC), FACTS devices, HVDC transmission systems necessitates the presence of Multilevel Inverter [1]. Multilevel inverter technology is based on the synthesis of a voltage waveform from several DC voltage levels. Various multilevel converters structures are reported in the literature, amongst them cascaded multilevel inverter appears to be superior to other multilevel inverter topologies in its application at high power rating due to the compact size, modularized circuit layout , control and reduced potential of electrical shock [3].

The growing demands of the industrial drives of high voltage needs the use of increasing level of Multilevel level inverter whose size is bulky due to the individual DC source and large number of switching units, causing increased switching losses and harmonics .To meet a quality output across the load, it is very essential to reduce the DC sources, switching units as well as the harmonics [4].

PWM techniques are used to reduce the THD, order of the harmonics in the output voltage [4]. As several soft switching techniques are avail, the SPWM technique is used for its capability of reducing even the lower order harmonics which is the main counterpart in the power quality domain [5].

In recent years, industry has demanded for high power equipments, which today reaches to megawatts. Hence, medium and high voltage ac drive systems have been considered widely. Today, due to limitation of semiconductor devices to operate in high current and voltage ratings, it is difficult to connect a semiconductor switch directly to medium voltage networks of (2.3 – 6.9 kV) [11].

Received December 15, 2014; Revised April 30, 2015; Accepted May 17, 2015

2. Multilevel Inverter

A. Topologies of Multilevel Inverters

As the Multilevel inverters have tremendous interest in the power industry. They present a new set of features that are well suited for their use in reactive power compensation. They consist of a series of power semiconductor devices and capacitors, which generate voltages with stepped waveforms in the output. Nowadays the use of multilevel approach is believed to be promising alternative in such a very high power conversion processing system. The advantages of this multilevel approach include good power quality, better electromagnetic compatibility (EMC), low switching losses, and high voltage handling capability.

Table 1. Required Components for Various types of multilevel inverter

Inverter Configuration	Diode-Clamp	Flying-capacitors	Cascaded-inverters
Main switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-2)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)(m-2)/2	0

From the above table 1 it is clear that the Cascaded Multilevel inverter requires very less number of components than any other multilevel inverter topologies. So CMLI is preferred for several power system applications even it has large number of switches for its higher levels.

B. Cascaded Multilevel Inverter

A Cascaded multilevel inverter consists of a series of H-bridge inverter units as shown in figure 1. The general function of MLI is to synthesize a desired voltage from several separate DC sources, which may be obtained from batteries, fuel cells, solar cells. Each SDCS is connected to an H-bridge inverter.

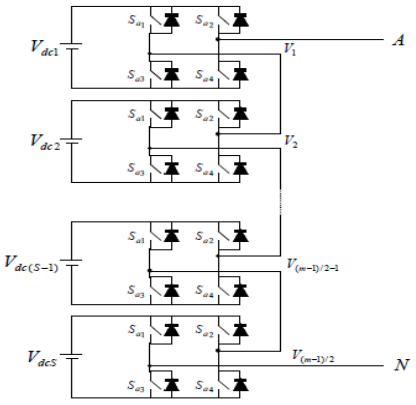

Figure 1. Conventional CMLI

The phase output voltage is synthesized by the sum of four inverter outputs from the equation (1).

$$V_{an}=V_{a1}+V_{a2}+V_{a3}+V_{a4} \quad (1)$$

3. Sinusoidal Pulse width Modulation

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse.

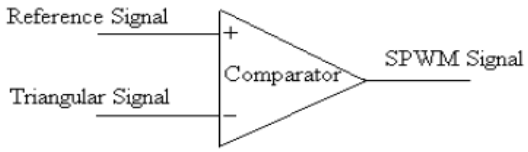

Figure 2. SPWM generator

Figure 2 is the SPWM generator where the gating signals are generated by comparing a sinusoidal reference signal Fr with a triangular carrier wave of frequency Fc. The frequency of reference signal Fr, determines the inverter output frequency and its peak amplitude Ar, controls the modulation index M, and RMS output voltage. The number of pulses per half cycle depends on carrier frequency.

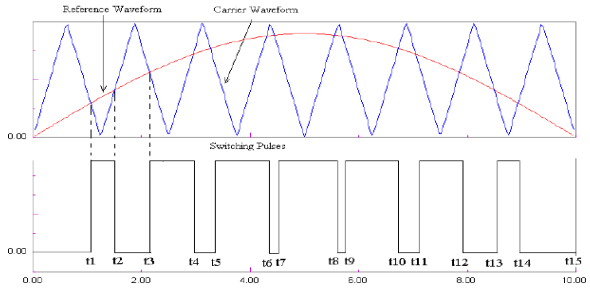

Figure 3. Sinusoidal Pulse width Modulatio

4. Methods of Reducing Switches and DC Sources

A. Method Used to Reduce DC Source

Symmetrical:

$$N_{step} = 2n+1 \quad (2)$$

$$V_{0max} = n \times V_{dc} \quad (3)$$

From the equation (2) & (3) the number of voltage levels and maximum output voltage for the proposed module can be calculated.

Asymmetrical:

N step =2n+1 -1 for n = even
N step =2n+1 for n = odd
V0max = (2n-1) ×Vdc (4)

where,

n is the number of bridges.
N_{step} is the output voltage levels.
V_{0max} is the maximum output voltage.

Among these two topologies of inverter the asymmetrical is preferred for its fewer requirements of switches and DC sources from the equation (2), (3), (4).

B. Methods of Reducing Switches

Table 2. Methods of reducing switches

TYPE	FIRST METHOD	SECOND METHOD	THIRD METHOD
No of MOSFETs	2n+2	2(N+1)	N+5
Source variety	1	2	4
Voltage drop	(n+1)/3	2(n+2)	3n

where,

n is the number of bridges.

N is the number of voltage levels.

Among these three methods [3], in the table 2 the first method is preferred because of its reduced switches, low voltage drop and the flexibility to operate in both symmetrical and asymmetrical MLI.

5. Method Preferred to Supress the Harmonic Level

Harmonic elimination technique is a method to get rid of harmonics by judicious selection of the firing angles of the inverter which is calculated by using either Newton Raphson Method or Gauss Siedel Method of Iterative Optimization. The harmonics elimination technique eliminates the need of expensive low pass filters which is being used in the system to reduce the higher order harmonics [4]. The harmonic elimination is computed from the Fourier Analysis of the produced voltage.

$$f(x) = a_0 + \sum_{n=1}^{\infty} \left(a_n \cos\frac{n\pi x}{L} + b_n \sin\frac{n\pi x}{L} \right) \quad (5)$$

From equation (5) the fundamental voltage of the produced output component is calculated.

where,

a_0=fundamental harmonic content.

a_n,b_n are harmonic constants of order n.

To eliminate the 5th, 7th, 9th order harmonics, the firing angles for each level is found by solving the following equations,

$$\begin{aligned}
&\frac{4V_{dc}}{\pi}\left(\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)\right) = h_1 \\
&\frac{4V_{dc}}{\pi}\left(\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4)\right) = h_5 \\
&\frac{4V_{dc}}{\pi}\left(\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4)\right) = h_7 \\
&\frac{4V_{dc}}{\pi}\left(\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4)\right) = h_{11}
\end{aligned} \quad (6)$$

where

V_{dc} is the input DC voltage.

θ_1,θ_2,θ_3,$\theta_4$are firing angles of various levels.

h_1,h_5,h_7,h_{11} are the harmonic order of 1,5,7,11respectively.

The modulation index is 1, since the voltage that has been used in these calculations is in per unit (p.u) from the nonlinear equations (6) firing angles for various harmonic levels will be calculated.

By solving the equation (6) using Newton Raphson Method, the switching angles for a 5-level and 9-level cascaded H-bridge multilevel inverters were calculated.

$$\theta_1 = 12.1260^0 \quad \theta_2 = 20.8465^0 \quad \theta_3 = 38.6570^0 \quad \theta_4 = 63.3546^0$$

By triggering the switches at the above cited delay angles, the harmonics of the load voltages are much reduced.

6. Results and Discussion

A. Simulink Model for Proposed Nine Level CMLI with SPWM

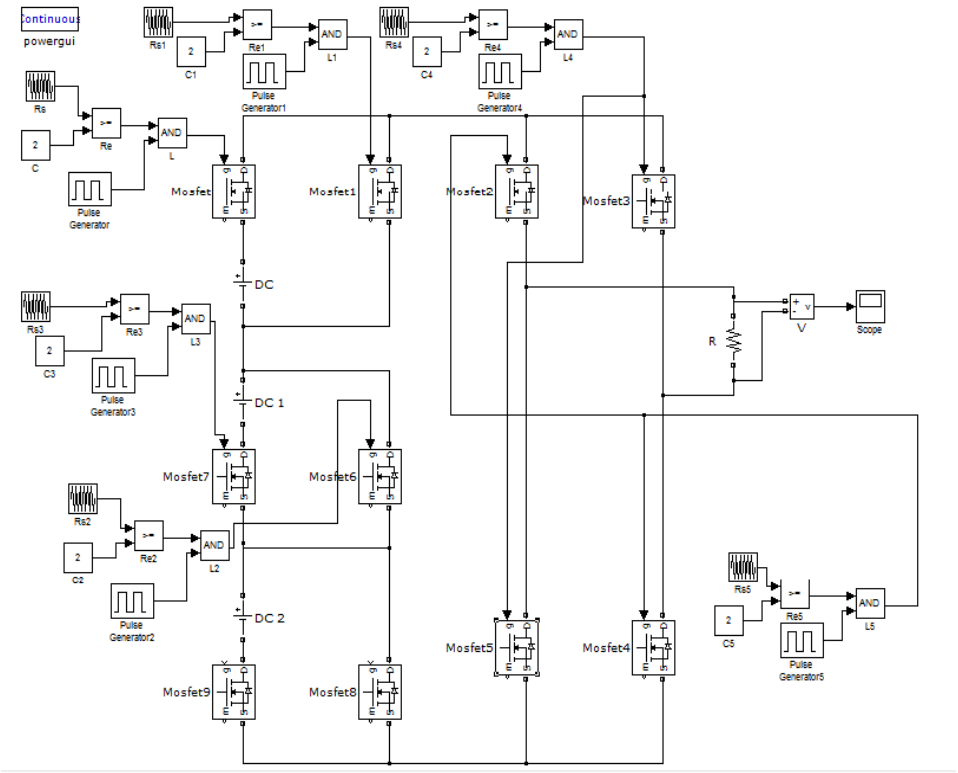

Figure 4. Simulink model of proposed nine level with SPWM

The simulation model of the proposed seven level inverter with SPWM technique is shown in the figure 4.The load chosen to connect across the proposed MLI is of pure resistive of 100Ω with the operating voltage of 100V and its is simulated for a time of 0.1sec.

1. Switching Sequence

Table 3. Switching sequence of nine level proposed CMLI.

VOLTAGELEVELS	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
$-4V_{dc}$	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON
$-3V_{dc}$	OFF	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF
$-2V_{dc}$	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
$-V_{dc}$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
V_{dc}	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
$2V_{dc}$	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
$3V_{dc}$	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
$4V_{dc}$	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF

The table 3 shows the appropriate time at which the MOSFETs to be switched ON and OFF. Here the switches T_1, T_3, T_5 connected across the positive supply which conducts only during the positive half cycle whereas switches T_2, T_4, T_6 conducts during negative half cycle. The switches in a common leg T_7 to T_{10} will conduct in both the positive and negative half cycles.

2. Output Voltage Waveforms

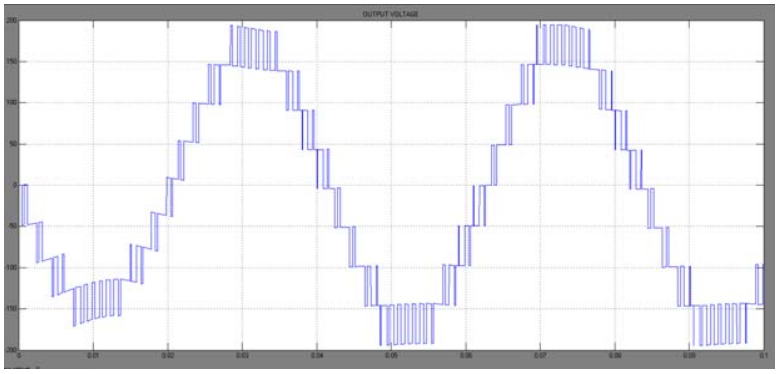

Figure 5. Voltage waveform of nine level proposed CMLI with SPWM

In figure 5 shows the output of the nine level proposed CMLI with SPWM technique whose pulses are of unequal width which reduces the harmonics of the output voltage. The SPWM reduce the lower order harmonics of the output voltages.

3. FFT Analysis

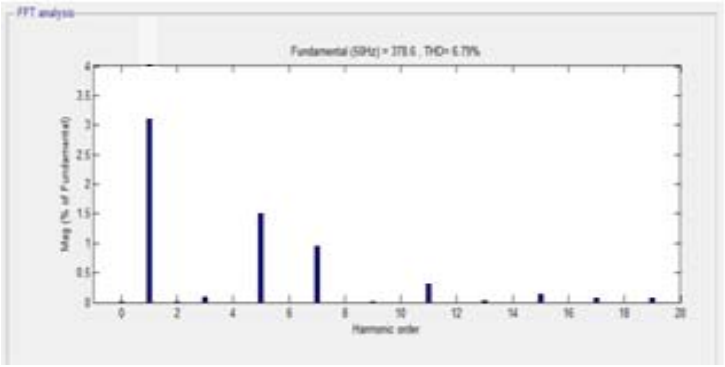

Figure 6. FFT Analysis of nine level with SPWM

Figure 6 is the FFT analysis with the reduction of harmonics by the harmonic reducing angles. The Total Harmonics Distortion of seven level without SPWM is 6.79%

B. Simulink Model of Proposed Nine Level CMLI without PWM

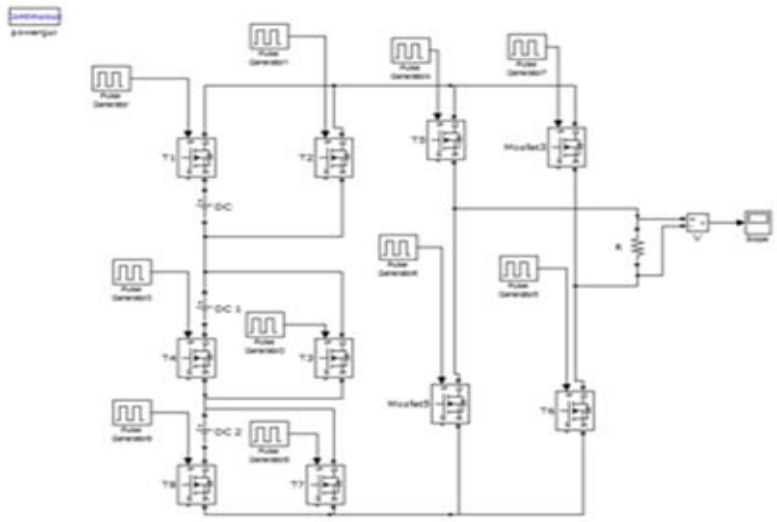

Figure 7. Simulink model of proposed nine level CMLI without PWM

The simulation model of the proposed seven level inverter with PWM technique is shown in the figure 6.9. The load chosen to connect across the proposed MLI is of pure resistive of 100Ω with the operating voltage of 100V Here the pulse generator is used to trigger the switches.

1. Output Waveform

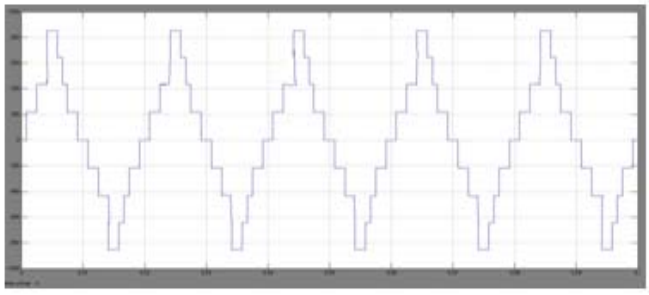

Figure 8. Output waveform of proposed nine level CMLI without PWM

Figure 8 is the output voltage waveform of the proposed CMLI without SPWM. Due to reduction of switches the output voltage waveform is somewhat distorted but the harmonic level is much reduced. The pulse generators are switched at the harmonic reducing angles.

2. THD Analysis

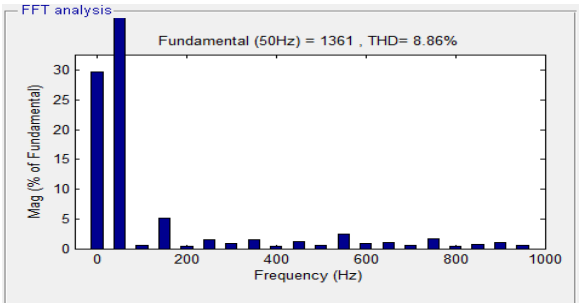

Figure 9. FFT Analysis

Figure 9 is the FFT analysis with the reduction of harmonics by the harmonic reducing angles. The Total Harmonics Distortion of seven level without SPWM is 8.86%**.**

7. Comparitive Study of Proposed CMLI and Conventional Model

A. Physical structure

DC Source

The number of DC source is directly proportional to the number of auxiliary bridges used in the proposed CLMI.

SEVEN LEVEL: Two DC sources are used instead of three as in conventional CMLI.

NINE LEVEL: Three DC sources are used instead of four as in conventional CMLI.

Number of switches

Table 4. Comparison of Number of switches

Number of Levels	Five	Seven	Nine
Conventional	8	12	16
Proposed	6	8	10

Table 4 shows the reduction switches in the proposed model of CMLI than in the conventional model.

B. Comparision of THD

Table 5. Comparison of THD values

OUTPUT VOLTAGE LEVELS	CONVENTIONAL CMLI	PROPOSED CMLI	
		WITHOUT PWM	WITH SPWM
SEVEN	40.07	20.69	19.09
NINE	32.1	8.86	6.79

Table 5 shows the percentage of THD values of various voltage levels in which with PWM the THD values are reduced while comparing with non-PWM values of THD.

In the proposed model each level is increased by increasing two switches of each bridge instead of four switchs. The voltage across the main and auxiliary bridge is in the ratio of 1:no of bridges(N).The separate DC source neccesity is overcomed by the new proposed model which favours the use of CMLI in high power drive applications.

8. Conclusion

The new topology of cascade multilevel inverter with reduced switches and DC sources have been proposed for nine level of output voltage. The benefit of this model includes the reduction of cost of converter station and DC source. The Harmonic levels are further reduced by using the soft switching techniques. The THD for various levels and the physical structure of the conventional versus proposed CMLI is analyzed and compared using MATLAB 8.0 Simulink environment. Thus this proposed work overcomes the disadvantages of conventional cascaded multilevel inverter.

Future Scope

For the advent of medium and high power system applications, the proposed CMLI is modeled with some power system components such as STATCOM, PD and PID controllers the switching losses and the harmonics are eliminated. It also used to control the AC and DC motor drives, HVDC transmission systems.

Future Work

The proposed model is further developed for higher levels and the THD values can be reduced by using some special switching techniques like Fuzzy Logic Theory, PI & PID Controllers, Space Vector Modulation etc.

References

[1] Rohan Ali Ahmed, S Mekhilef. "New multilevel inverter topology with minimum number of switches". *IEEE transaction on power electronics*. 2010.
[2] G Mahesh. "Simulation of Cascaded multilevel inverter with less number of Switches". *Applied Science*. 2011
[3] Babaei E, Hosseini SH. "New cascaded multilevel inverter topology with minimum number of switches". *Energy conservation & management*. 2009; 55.
[4] Babaei E, Hosseini SH. "New inverter topology with less number of switches". *IEEE Journal*. 2011; 45.
[5] Zhongdu, Tolbert. "*A Cascaded multilevel inverter with single DC source*". In Proc IEEE APEC'06. pp 426-430.
[6] C Liu, B Wu, N Zargari, and D Xu. "A novel nine-switch PWM rectifier-inverter topology for three-phase UPS applications". *EPE J*. 2009; 19(2).
[7] Mohamud Rashid. "Power Electronics". Prentice Hall of India Second Edition. 2004
[8] C Liu, B Wu, N Zargari, and D Xu. "A novel three-phase three leg AC/AC converter using nine IGBTs". *IEEE Trans. Power Electron*. 2009; 24(5): 1151–1160.
[9] SM Dehghan, M Mohamadian and A Yazdian. "Space Vectors Modulation for Nine-Switch Converters". *IEEE Energy Conversion Congress and Exposition (ECCE)*, California, USA. 2009.
[10] A Subbiah. "A Comparative Study of Pulse Width Modulation Techniques". *International Journel of Scientific and Engineering Reasearch*. 2010; 1.
[11] Abelhamid, Tamer, Jamal, "Advanced three-phase multilevel inverter with least number of devices operating from non-equal DC source". *International*. 2008.
[12] JNChiasson, LM Tolbert, K McKenzie, Z Du. "Harmonic Elimination in Multilevel Converters". *IASTED International Conference on Power and Energy Systems (PES 2003)*. Palm Springs, California, 2003: 284-289.
[13] JS Lai, FZ Peng. "Multilevel Converters - A New Breed of Power Converters". *IEEE Transactions on Industry Applications*. 1996; 32(3): 509-517.
[14] FZ Peng, JW McKeever, DJ Adams. "A Power Line Conditioner Using Cascade Multilevel Inverters for Distribution Systems". *IEEE Transactions on Industry Applications*. 1998; 34(6): 1293-1298.
[15] LM Tolbert, FZ Peng, TG Habetler. "A Multilevel Converter-Based Universal Power Conditioner". *IEEE Transactions on Industry Applications*. 2000; 36(2): 596-603.
[16] JN Chiasson, LM Tolbert, K McKenzie, Z Du. "A Complete Solution to the Harmonic Elimination Problem". *IEEE Applied Power Electronics Conference (APEC 2003)*. Miami, Florida. 2003: 596-602.
[17] N Mohan, TM Undeland, and WP Robbins. Power Electronics: Converters, Applications, and Design. Second Edition. John Wiley and Sons. 1995.
[18] JN Chiasson, LM Tolbert, KJ McKenzie, Z Du. "Control of a Multilevel Converter Using Resultant Theory". *IEEE Transactions on Control System Theory*. 2003; 11(3): 345-354.
[19] FS Shyu and YS Lai. "Virtual Stage Pulse-Width Modulation Technique for Multilevel Inverter/Converter". *IEEE Transactions on Power Electronics*. 2002; 17: 332-341.
[20] JN Chiasson, LM Tolbert, KJ McKenzie, Z Du. "A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters". *IEEE Transactions on Power Electronics*. 2004.
[21] JN Chiasson, LM Tolbert, KJ McKenzie, Z Du. "Control of Cascaded Multilevel Converters with Unequal Voltage Sources for HEVs". *IEEE International Electric Machines and Drives Conference*, Madison, Wisconsin. 2003: 663-669.
[22] LM Tolbert, FZ Peng. "Multilevel Converters as a Utility Interface for Renewable Energy Systems". *IEEE Power Engineering Society Summer Meeting*, Seattle, Washington. 2000: 1271-1274.