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High-performance Cuk converter with turn-on switching at zero voltage and zero current

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ABSTRACT

The soft-switching technique has the potential to significantly enhance the performance of the power converter. This is primarily because it allows for an increase in the switching frequency, which ultimately leads to improved modulation quality. This raises extra concerns, particularly in high-power applications, because in a standard hard-switching converter structure, components can often not function at frequencies higher than a few hundred hertz. This paper presents a high-efficiency soft switching CUK converter. When the main and auxiliary switches are turned on and off at zero voltage, the proposed converter yields zero voltage and zero current. The suggested method is ideal for a DC-DC converter based on IGBTs or MOSFETs. The recommended systems are described using theoretical analysis, the results of computer simulations, and experimental data derived from a prototype. The design parameters of the inductance and capacitor circuit for edge-resonant soft switching were obtained using the output power and the switching duty ratio. In the end, soft-switching is better than hard-switching in terms of efficiency, particularly when operating under full load.

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1. INTRODUCTION

Power supply for personal computers, office equipment, spacecraft power systems, laptop computers, telecommunications equipment, as well as DC motor drives, all make use of DC-DC power converters. A soft-switched pulse-width modulation (PWM) converter, high-power applications-appropriate, has been presented [1]. High power density and high efficiency can be obtained from them, because the commutation takes place under zero-voltage or zero-current.

To lessen switching losses and electromagnetic (EM1) sounds, Cuk converters have been frequently employed as LED drivers [2]–[4]. In other words, a Cuk converter has substantially greater power handling requirements for its semiconductor components than a similar output power may be achieved using either a buck converter or a boost converter. A Cuk converter places a lot of emphasis on lowering the switching losses and increasing the EM1 sounds [5]. Designing a soft switching converter is extremely difficult because of the strict limitations on the permitted current/voltage stress and conduction losses. The fact that the converter is being fed with DC as an input just serves to increase the challenge of finding a solution. It is well known that, for soft switching, a non-zero product of the switch's voltage and current must accompany the switching transition, and that, to prevent the voltage and current from canceling each other out in a DC-DC converter, a sub-circuit containing active and passive switches and resonant devices must be specially

designed [6]. Resonant elements aid in bringing the current/voltage of a switch to zero before a switching transition, consequently, the switch is subjected to high current/voltage stresses.

The constant aims of switching-mode power supply development have been high efficiency and compact size [7]–[10]. Large switching losses were being produced by the traditional hard-switching PWM converters. Quasi-resonant converters (QRC) were able to minimize the size and weight of the circuit by using a soft-switching approach that minimized switching losses and allowed for high frequency operation. Another type of high step-up DC-DC converter is non-isolated converters. Because of their simplicity, small size, low cost, and great efficiency, non-isolated converters have a wide range of applications. The conventional boost converter is modified to increase high-voltage gain and efficiency. A high voltage conversion ratio could be attained using the coupled-inductor method. The turns ratio of the coupled inductor is a second factor that affects how well a boost converter with a coupled inductor operates in terms of controlling the voltage gain [11], [12].

As a result, a high-voltage gain is simple to accomplish. Another benefit of these topologies is the reduced voltage stress that power switches experience. Regarding the drawbacks of these converters, the coupled inductor's coupled turn ratio increases the leakage inductance, which can result in issues such voltage spikes and strains across the power switches. Using active [13], [14], and passive clamp [15], [16] circuits reduce voltage spikes on the power switch, but the converter construction has become more complicated and expensive. Using a clamping circuit is thought to have the benefit of providing zero-voltage-switching (ZVS) or zero-current switching (ZCS) conditions for the power switches. Another way to increase the conversion ratio and efficiency of high step-up DC-DC converters is by using the switched-capacitor (SC) technique [17], [18]. These converters produce high-voltage gain by charging the capacitor in parallel with the input voltage and delivering the stored energy in the series to the load. Conduction losses rise as a result, however the semiconductor elements will experience high transient current [19].

Switching losses of power semiconductors account for a significant proportion of all losses in DC-DC converters. In order to offer the necessary step-up of renewable energy sources with the best power efficiency, many different soft-switched step-up architectures have been developed. However, a number of hard-switched step-up architectures have been proposed in various works, and all of these designs exhibit significant power semiconductor switching losses [20]–[25].

This article describes the development of the novel Cuk converter, which offers zero capacitive turn-on losses due to the converter's sophisticated design and ZVS at the commutation of the active device, for a wide line and load range of switches and recovery diode. The Cuk version was chosen because it could make voltages that were equal to or higher than the voltage that was put in. With the switch voltage stress being lower than the output voltage, the voltage conversion ratio is also increased. Power conversion efficiency is increased as a result of low-voltage stress and switching device ZVS and ZCS operation. In-depth discussions are held on the suggested converter's design parameters, theoretical analysis and characterization, and operating principle. The suggested converter's performance is then checked by testing the experimental prototype and running simulations.

2. CONVERTER PROPOSAL ANALYSIS

The proposed converter is intended to provide ZVS (ZCS-ZVS) to the primary switch. This is achieved by integrating additional components into the conventional converter. The auxiliary component must also switch under ZCS-ZVS by itself, verifying that no additional switching loss occurs during the building of the ZVS circuit. The suggested PWM zero-voltage-transition (ZVT) Cuk converter is depicted in Figure 1. The auxiliary devices S_1, C_1, D_3, L_r, and D_4 create the subsequent to provide a favourable switching state for the main device S_2, while Lr and C_1 form the resonant tank to provide ZVS switching. The link formed by D_3 and L_r is used to remove the charge across S_2 in order to provide the ZVS condition. C_2 is connected in parallel with the primary switch S_2 to give ZVS when the switch is turned off.

In one switching cycle as in Figure 2, the proposed CUK converter passes through seven topological phases, which are seen in Figure 3, respectively. Multiple assumptions are established during each switching cycle to facilitate the investigation of operation stages [a, g]; i) all of the circuit's components are typical, ii) the inductors for both the input and output filters, L_{fi} and L_{fo}, are sufficiently large that the filters, I_{in} and I_o, can be treated as constant current sinks, iii) because the output capacitors C_{01} and C_{02} are large enough, their voltages are set as V_o and V_{C02}, and they may be represented as constant voltage supplies, and iv) the input voltage, V_i, is fixed.

DC resistances of inductors, and transistor on-resistances are all calculated. Forward voltage drops of diodes are not taken into account because the goal of the study is to discover a straightforward, strategy based on design. Figure 2 shows how the active switches are operating. In Figure 2, and the main switch S_2 was turned off. Input and output current were carried by the rectifier diode D_o, the converter's theoretical

steady-state main waveforms are also depicted. As a result, each cycle of the converter has seven switching stages (a-g). Prior to the beginning of a new cycle, the auxiliary switch S_1 was switched on while D_3 carried a constant-value inductor current (I_{in}+I_o).

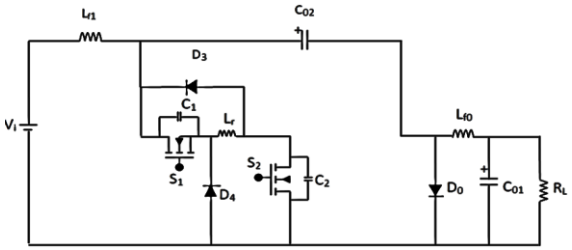

Figure 1. Schematic of the proposed PWM ZVT CUK converter

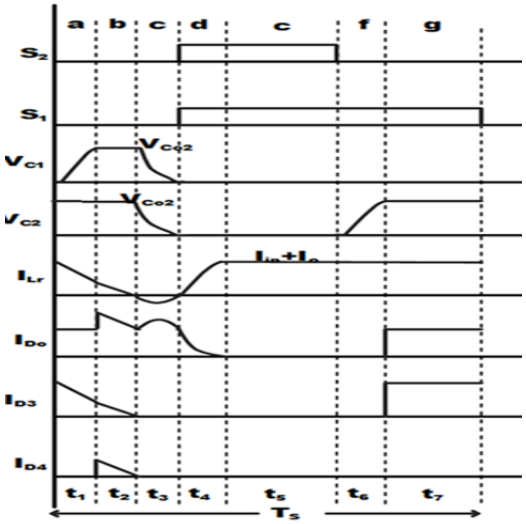

Figure 2. The suggested converter's key waveforms

2.1. Stage a: C_1-capacitor charging (t_0-t_1)

When S_1 is turned off by the clock signal, a new cycle begins. As it approaches V_{C02}, the voltage across the parasitic capacitance S_1 increases (before being clamped by D_4). Do keeps carrying the combined input and output current. By resolving the linear circuit of Figure 3(a). The converter waveforms' expressions are discovered.

$$\begin{aligned} V_{C1}(t) &= Z_1(I_{in} + I_o)sin\omega_1 t \\ i_{Lr}(t) &= (I_{in} + I_o)cos\omega_1 t \\ V_{C2}(t) &= V_{C02} \end{aligned} \quad (1)$$

Where:

$$Z_1 = \sqrt{\frac{L_r}{C}} \text{ and } \omega_1 = \frac{1}{\sqrt{L_r C}} \quad (2)$$
$$C = C_1 = C_2$$

S_1 and S_2 were considered to be identical switches. The initial conditions are as shown in:

$$VC1(0) = 0, VC2(0) = VC02, ILr(0) = Iin + Io$$

And the final conditions are:

$$VC1\ (t1) = VC2\ (t1) = VCo2,$$

$$I_{Lr}(t) = (I_{in} + I_o)\sqrt{1-\propto}$$

With

$$\propto = \frac{V_{Co2}}{Z1(I_{in}+I_o)}$$

indicating the length of the first stage as (3).

$$t_1 = \frac{\sin^{-1}\propto}{\omega_1} \quad (3)$$

V_{D4} equals 0 and D_4 is switched on with ZVS when V_{C1} reaches V_{C02}. Indicators of the commutation include zero capacitive turn-on losses.

2.2. Stage b: discharging of a resonant inductor (t_1-t_2)

The inductor current I_{Lr} is discharged along the link D_o-V_{C02}-D_3-L_r-D_4 until it reaches zero. D_o passes all of the current (I_{in}+I_o+I_{D3}). This phase, which is seen in Figure 3(b), is crucial to the converter design. A resonant inductor current peak is prevented by discharging the inductor before the multi resonance stage. The waveform expressions are as (4).

$$\begin{aligned} &V_{C1}(t)=V_{C02},\\ &V_{C2}(t)=V_{C02}\\ &I_{Lr}(t) = (I_{in} + I_o)\sqrt{1-\propto} - \frac{V_{Co2}}{L_r}\\ &V_{C1}(t_2)=0,\ V_{C2}(t_2)=0,\ I_r(t_2)=0 \end{aligned} \quad (4)$$

When the stage is complete. The duration of the stage as (5).

$$t_2 = \frac{(I_{in}+I_o)\sqrt{1-\propto}}{V_{Co2}} L_r \quad (5)$$

D_3 and D_4 are naturally switched off when I_L is zero.

2.3. Stage c: three-element resonance (t_2-t_3)

At this stage Figure 3(c) is. When Lr, C_1 and C_2 resonant, V_{C1}, V_{C2} and I_{Lr} simultaneously go to zero. This circumstance causes S_1 and S_2 to switch on at zero voltage and zero current. Unlike other converters discussed in the literature, the switches do not experience capacitive turn-on loss, because they are only activated when the current and voltage are zero. The following list includes the current and voltage expressions.

$$\begin{aligned} &V_{C1}(t) = V_{C2}(t) = \frac{V_{Co2}}{2}(\cos\omega_e + 1)\\ &I_{Lr}(t) = -\frac{V_{Co2}}{Z_e}\sin\omega_e\\ &I_{Do}(t) = (I_{in} + I_o) - I_{Lr}(t) \end{aligned} \quad (6)$$

Where:

$$C = C1 = C2 \text{ and } \omega_e = \frac{1}{\sqrt{L_r\left(\frac{C}{2}\right)}} \quad (7)$$

The duration's end is established as (8)

$$VC1(t3) = 0, VC2(t3) = 0, Ir(t3) = 0$$

$$t_3 = \frac{\pi}{\omega_e} \quad (8)$$

The largest absolute value of I_{Lr} at this stage as (9).

$$I_{Lr\_max} = \frac{V_{Co2}}{Z_e} \quad (9)$$

Since C is a parasitic capacitance of nF order, L >> C suggests that (9). At this time, the flow of current via D_o as (10).

$$I_{Do}(t) = (I_{in} + I_o) + \frac{V_{Co2}}{Z_e} sin\, \omega_e \quad (10)$$

With

$$I_{Do\_max} = (I_{in} + I_o) + \frac{V_{Co2}}{Z_e} \quad (11)$$

The only switch in the proposed circuit to experience overload in this way is this one. However, since (9) is so little, this pressure does not need an increase in the D_o rating.

2.4. Stage d: resonant inductor charging (t_3-t_4)

As illustrated in Figure 3(d), the first thing that happens is that S_1 and S_2 are activated by ZVS. The commutation has no turn-on capacitive losses. A linear rise in inductor current occurs until it in this phase.

$$VC1(t) = 0, VC2(t) = 0, I_{Lr}(t) = \frac{V_{Co2}}{L_r} t \quad (12)$$

With the final conditions.

$$VC1(t4) = 0, VC2(t4) = 0,$$

$$I_{Lr}(t_4) = (I_{in} + I_o)$$

Giving the interval duration as (13):

$$t_4 = \frac{(I_{in}+I_o)L_r}{V_{Co2}} \quad (13)$$

As $I_{Do} = (I_{in} + I_o) - I_{Lr}$.

When the duration reaches zero, I_{Do} also goes to zero, and D_o automatically turns off.

2.5. Stage e: controlled (t_4-t_5)

During this stage as in Figure 3(e).

$$VC1(t) = 0, VC2(t) = 0, ILr(t) = Iin + Io \quad (14)$$

During this duration, the input is disconnected from the output, and a steady current flow from the input filter inductor and the output filter inductor to the resonant inductor L_r. The duration of this stage is controlled by the feedback loop to regulate the output voltage as (15).

$$D = \frac{t_5}{T_s} = \frac{V_o}{V_o - V_i} \quad (15)$$

2.6. Stage f: capacitor charging (t5-t6)

Stage "f" operation begins when S_2 is opened at ZVS to begin charging C_2 at a constant current, as indicated in Figure 3(f). Diodes D_3 and D_o conduct to terminate the current stage when V_{C2} equals V_{C02}.

$$v_{C2}(t) = \frac{(I_{in}+I_o)t}{C_2}$$

$$i_{Lr}(t) = (I_{in} + I_o) \quad (16)$$

$$i_{Do}(t) = 0$$

At the end of this stage $v_{C2}(t_6)$=V_{C02} and the duration as (17).

$$t_6 = \frac{V_{Co2}C_2}{(I_{in}+I_o)} \quad (17)$$

2.7. Stage g: freewheeling mode (t6-t7)

During this phase, as seen in Figure 3(g), the energy stored in the filter inductor is transferred to the output capacitor and load while the current in L_r freely circulates via D_3 and S_1. The duration's conclusion is dictated as (18).

$$VC1(t7) = 0, VC2(t7) = VCo2$$

$$ILr(t7) = Iin + Io, IDo(t7) = Iin + Io \quad (18)$$

This description of a converter allows for soft switching without any losses due to capacitive turn-on. The extra conduction loss on switch S_2 is the cost of this achievement. However, S_2 is only used in two stages, reducing losses significantly.

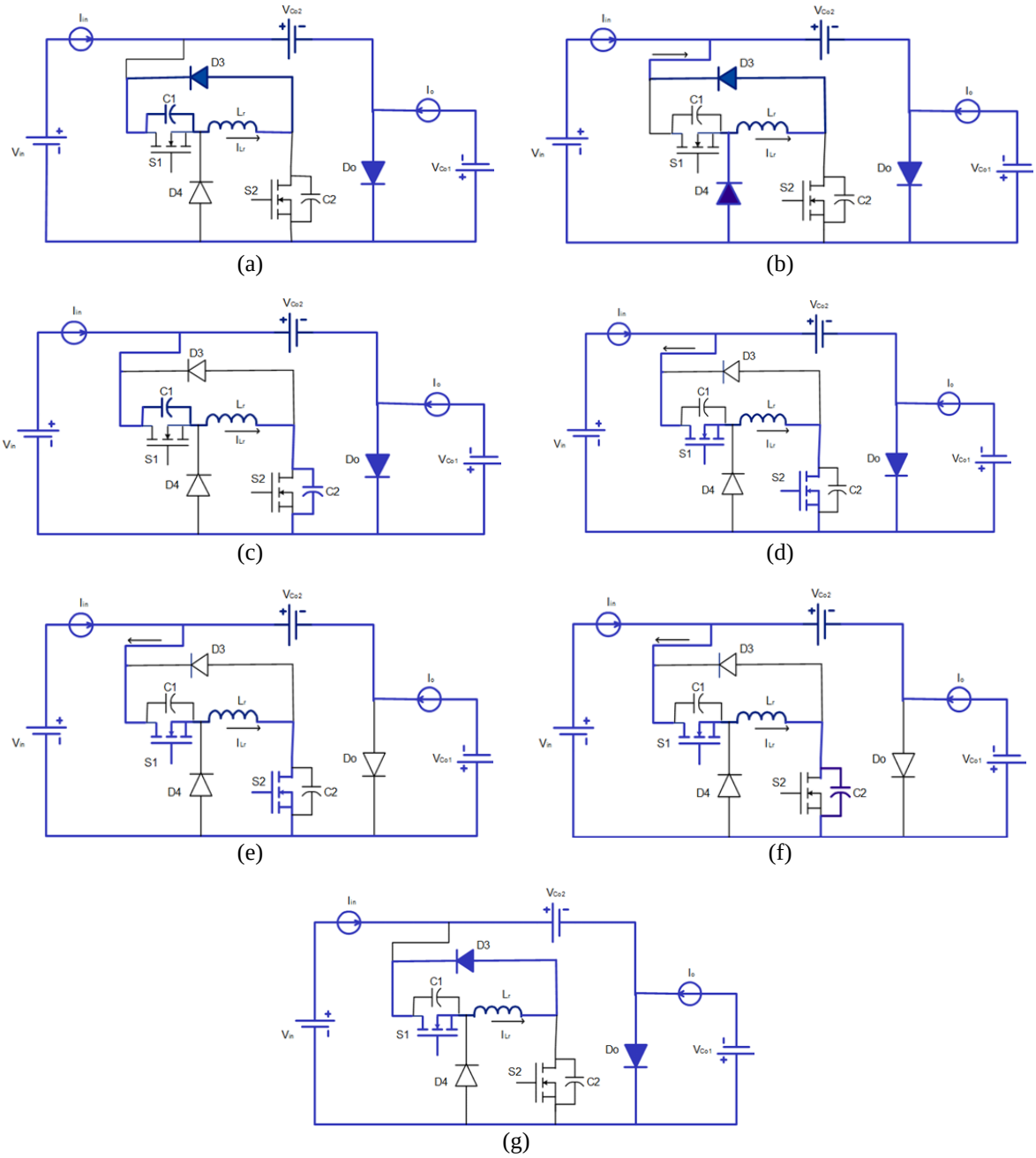

Figure 3. The Cuk converter's stages; (a) C1-capacitor charging, (b) resonant inductor discharging, (c) three-element resonance, (d) resonant inductor charging, (e) controlled stage, (f) C2-capacitor charging, and (g) free-wheeling stage

3. CHARACTERISTIC AND DESIGN PARAMETER

Using the output power and switching duty ratio, we can derive the values for L_{fo}, L_{f1}, L_r, C_1, C_2, C_{01}, and C_{02} in the circuit design of the edge-resonant modules. This section provides a description of the resonant modules L_r and C_1 to demonstrate a design principle. The highest output power $P_{o\text{-}max}$ and the associated duty ratio D_{max}, as well as the lowest output power $P_{o\text{-}min}$ and the related duty ratio Dmin, are utilized to derive the circuit design parameters L_r and C_1. For edge-resonant soft-switching, the output power is varied from $P_{o\text{-}min}$ to $P_{o\text{-}max}$. The maximum time for soft switching at an edge resonance, denoted by tmax, is equal to DmaxTs. When the resonant capacitors C_1 and C_2 are discharged to zero and the switches S_1 and S_2 are activated, the minimal edge-resonant soft-switching time tmin occurs. Therefore, the minimal output power, $P_{o\text{-}min}$, may be used to determine the value of the resonant capacitors C_1 and C_2. One switching period T_s must be greater than $S_{1\text{-}min}$, the minimum time required for the complete discharge of the resonant current, in order to accomplish soft-switching commutation. Calculating the minimum time required for a complete discharge, $S_{1\text{-}min}$ [4], allows one to determine the resonant inductor L_r.

The capacitor voltages V_{C1} and V_{C2} must be drained to zero at the end of stage "c" in order to provide a condition for ZVS, and this is possible if V_{C1}=V_{C02} at the end of stage "a". It may be shown that both of the aforementioned requirements can be met if:

$$L_r > \frac{(V_{co2,max})^2}{(I_{in}+I_{o,min})^2} C \tag{19}$$

Which provides the L_r design value.

4. SIMULATION RESULTS

In Figure 4, a MATLAB/Simulink circuit for the CUK converter is shown with simulation of the mentioned circuit run with the following parameters: A constant current source sink was modeled for L_{f1} with V_{in}=12 V, V_o=-24 V, Iin=2 A, I_o=2 A, L_r=15 µH, C_1=C_2=20 nF, Lfo=300 µH, C_{01}=250 µf, C_{02}=100 µf, and a switching frequency of f_s=100 kHz. The outcomes obtained via Simulink are shown in Figures 5 and 6, respectively. Because V_{C1}, V_{C2}, and I_{Lr} all reach zero before S_1 and S_2 are switched on, the MATLAB simulation makes it very evident that neither S_1 nor S_2 have any voltage or ZCS before they are turned on.

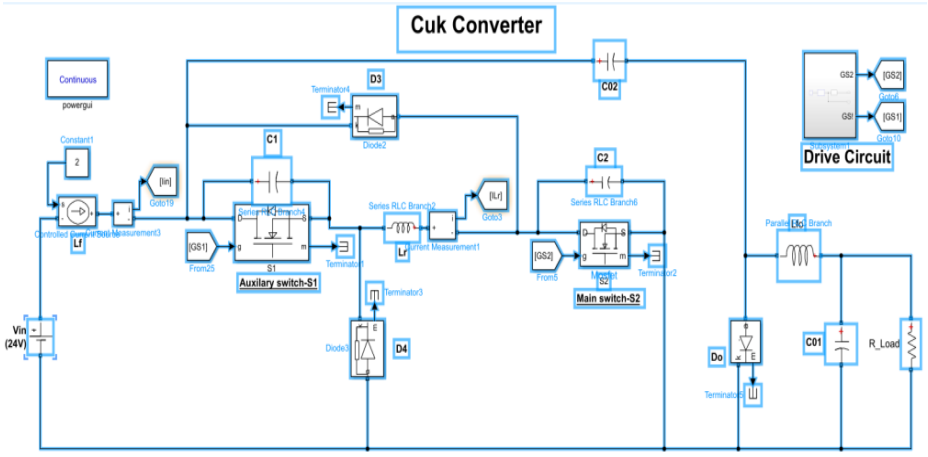

Figure 4. The MATLAB/Simulink CUK converter circuit

Figures 5(a) and (b) depicts the operating times of the main and auxiliary switches, as well as how they maintain synchronisation throughout the switching cycle.Before displaying the ZVS situation, Figures 5(c) and (d) shows the charging and discharging cycles of capacitors C1 and C2, as well as the simultaneous arrival of their respective voltages at zero. The currents for the inductor Lr, the diodes D3, D4, and the diode Do are shown in Figures 6 (a)-(d), respectively. The outcomes of the simulation are perfectly in line with the theoretical analysis presented in Section 2. The MATLAB simulation clearly shows that neither S1 nor S2 have any voltage or ZCS prior to being turned on because V_{C1}, V_{C2}, and I_{Lr} have all reached zero before S1 and S2 are turned on. The V–I curves of the two switches are shown in Figures 7(a) and (b), they demonstrate that both S_1 and S_2 operate in soft switching, just as the simulation in Matlab predicted they would.

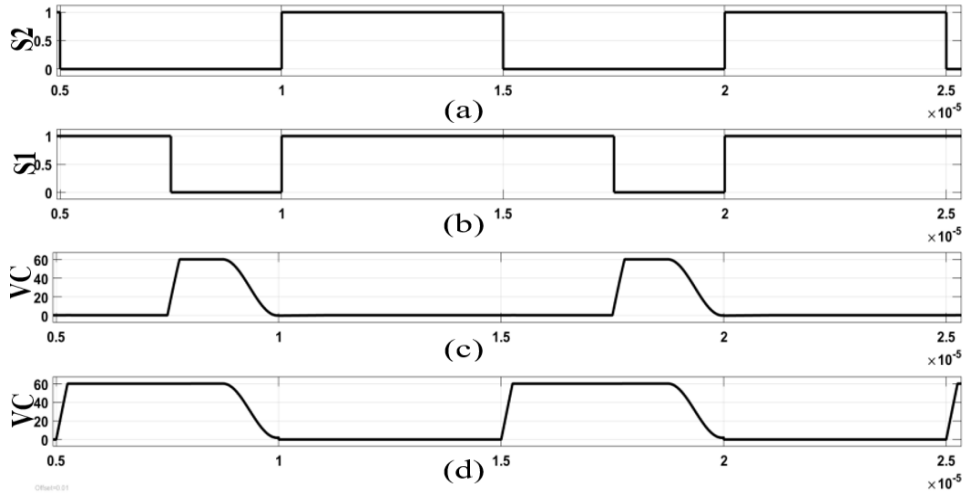

Figure 5. Simulation results of the Cuk converter (a) gate of the switch S2, (b) gate of the switch S_1, (c) voltage capacitor C1, and (d) voltage capacitor C2

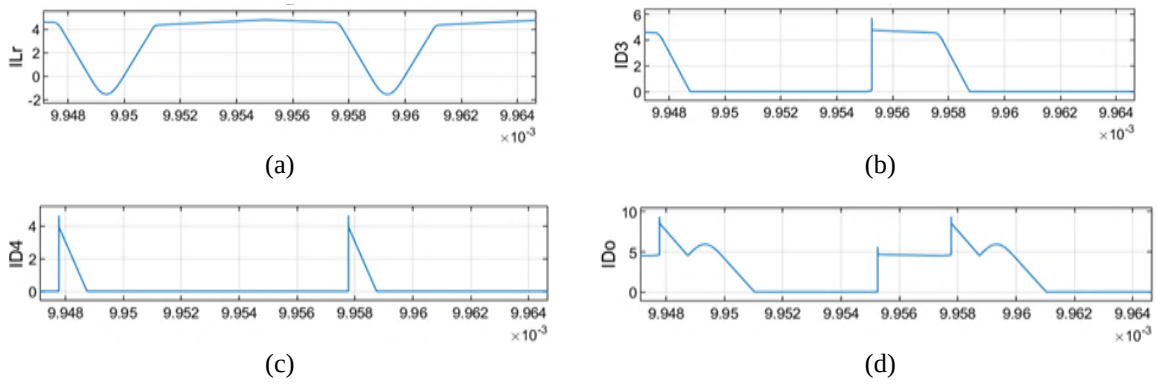

Figure 6. Simulation results of the Cuk converter (a) current inductor Lr, (b) current diode D3, (c) current diode D4, and (d) current diode Do

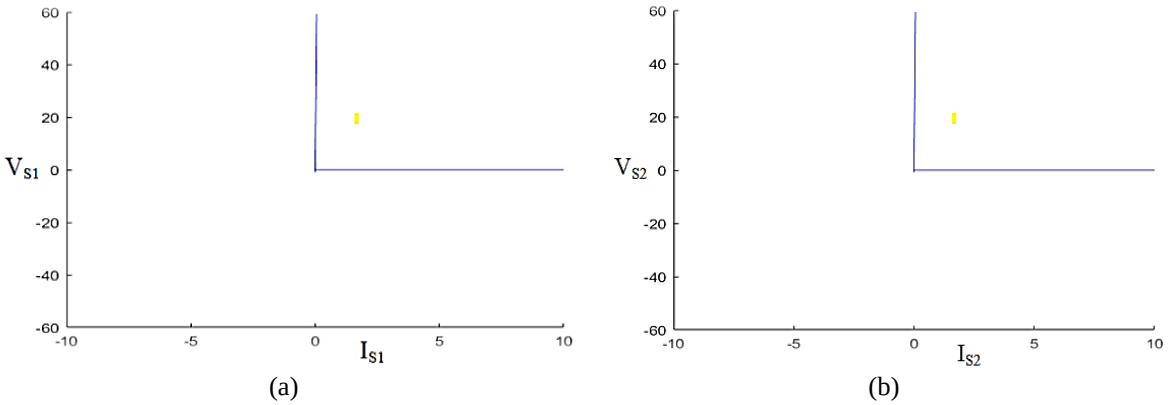

Figure 7. The switching trajectories of S_1 and S_2 (a) V-I diagram of S_1 and (b) V–I diagram of S_2

5. EXPERIMENTAL RESULTS

In the laboratory, a prototype was constructed with the following requirements and constraints: V_{in}=12 V, V_o=(11.5-60) V; I_{in}=2 A; I_o=(1-6.3) A, L_r=15 µH; C_1=C2=20 nF, L_{fo}=300 µH, C_{01}=250 µf, C_{02}=100 µf; and the switching frequency f_s=100 kHz. MOSFETS model IRF542 and diode model MBR20100 were selected for use in the prototype. Figures 8-12 illustrate the experimental waveforms that

were acquired from the prototype. The results emphasize the ZVS and ZCS of S_1 and S_2 when V_{C1}, V_{C2}, and I_{Lr} all arrive to zero at the same time before S_1 and S_2 are switched on.

Figure 8 shows the main and auxiliary switches' working durations as well as how they remain synchronized throughout the switching cycle. The readiness to turn on the main switch is shown in Figure 9 after the arrival at zero of the inductances current I_{Lr} and the capacitive voltage V_{C2} is shown. Figure 10 depicts the charging and discharging cycles of capacitors C_1 and C_2 as well as the simultaneous arrival of their respective voltages at zero before illustrating the ZVS condition. Figure 11 shows the main switch's soft-switching operation, which occurs when the main switch S2 is turned on and the current inductance ILr hits zero. The capacitive voltage V_{C2} and the inductance current I_{Lr}, which begin to clamp to zero prior to the application of the gate voltages S_1 and S_2, are shown in Figure 12. S_1 and S_2 are able to turn on at zero voltage as a result. Additionally, S_1 and S_2's maximum voltages are clamped to V_{C1} and V_{C2}, as can be observed. The converter achieves excellent regulation for a change in input voltage in the range of 12–24 V and a change in load current of 1–6.3 A. It also has an efficiency of over 96% over the whole range of specifications for which it was designed.

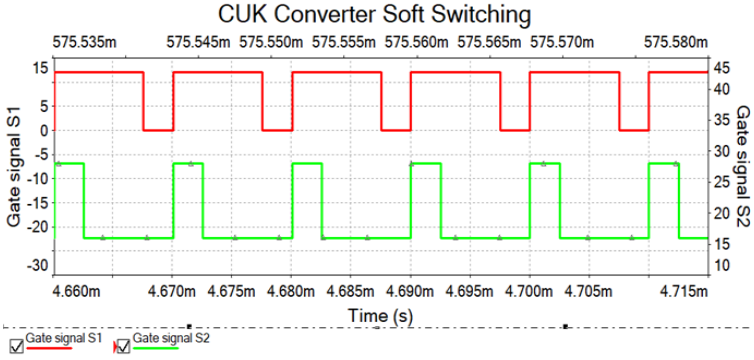

Figure 8. Experimental results of the gate signals to S_1 and S_2

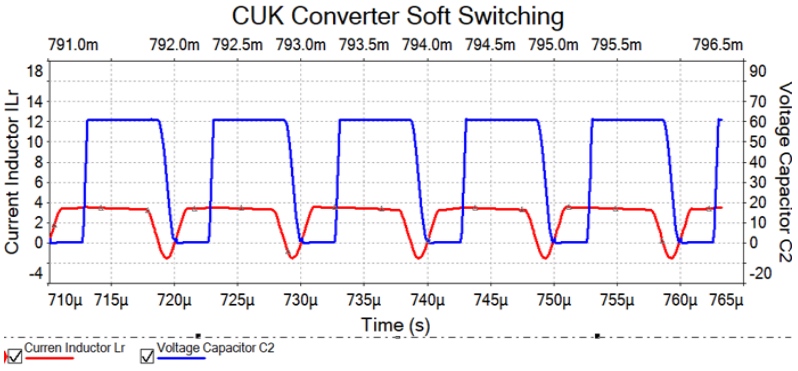

Figure 9. Experimental results of waveforms of V_{C2} and I_{Lr}

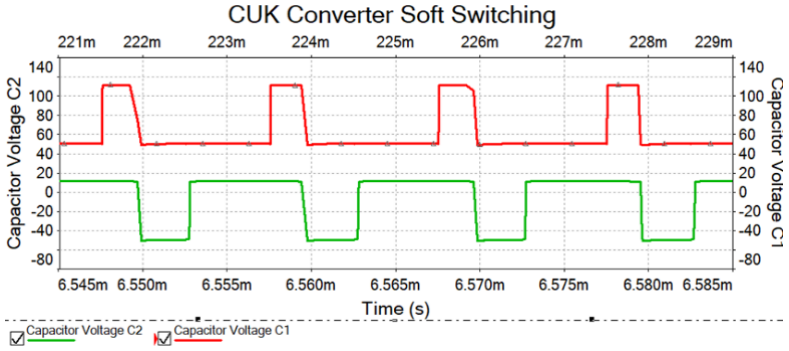

Figure 10. Experimental results of waveforms of V_{C2} and V_{C1}

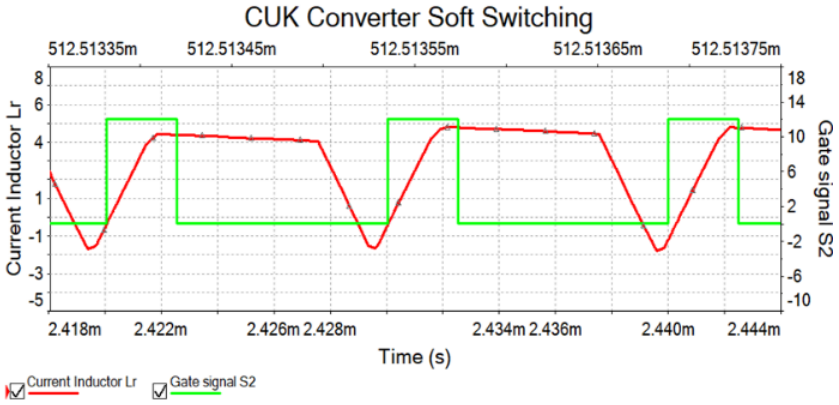

Figure 11. Experimental results of waveforms of I_{Lr} and S_2

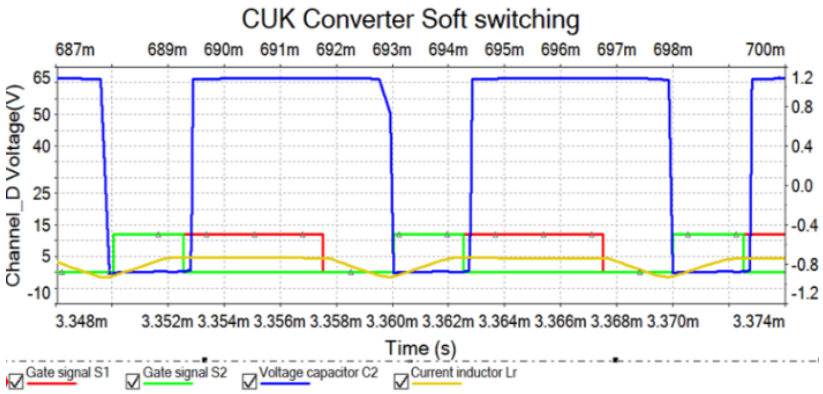

Figure 12. Experimental results of waveforms of S_1, S_2, I_{Lr} and V_{C2}

6. EFFICIENCIES AND POWER LOSS ASPECTS

The following formula can be used to calculate the overall power consumption losses of the proposed converter circuit.

$$P_{loss\_total} = P_{cond\_S2} + P_{sw\_S2} + P_{con\_S1} + P_{sw\_S1} + P_{con\_D3} + P_{sw\_D3} + P_{cond\_D4} + P_{sw\_D4} + P_{cond\_Do} + P_{sw\_Do} \quad (20)$$

In this regard, the energy losses of the inductor and capacitor parts have been omitted, and the losses of the auxiliary switch and diodes are considered to be minimal due to the brief duration of operation. When compared to a normal Cuk converter, there is no additional voltage stress delivered to the converter, therefore the main diode and switch do not experience an increase in their conduction losses [26]. This is the reason why there is no increase in the conduction losses of these components.

$$\eta = \frac{(P_{in-} - P_{loss\_total})}{P_{in}} \quad (21)$$

As can be shown in Figure 13, with maximum output power of 375 W and 100 kHz of the switching frequency, the new converter achieves an overall efficiency of 96%. The efficiency is nearly identical to that of a comparable converter described in [10], whose circuit works at 5 kW and 50 kHz nominally. Moreover, it can be shown that the efficiency levels are higher than those of most other SS converters, even at low output powers. As the load current decreases in the new converter, the converter loss likewise decreases, as it is very sensitive to recirculated energy. Finally, it was found that the theoretical analysis of the suggested ZVT–Cuk converter was perfectly confirmed by the simulation and experimental results.

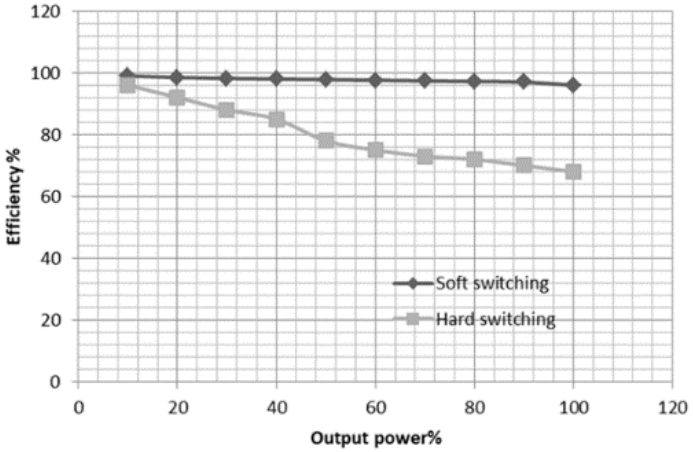

Figure 13. Comparing SS and HS converter efficiency curves

7. CONCLUSION

In this study, a novel edge-resonant Cuk converter is presented. Using simulation results, this study confirmed zero-voltage and zero- current turn on switching and zero-voltage during turn off switching in the commutation Cuk converter. The expert design of the Lr value allows the ZVS to be maintained throughout a large line and load range. The benefit of this converter is that it improves circuit power efficiency and decreases switch power loss. At high power and high frequency levels, a MOSFET-PWM converter is especially well suited to it. The suggested auxiliary circuit is also inexpensive, easy to operate, and has a simple construction. The converter with the suggested auxiliary circuit can run smoothly with soft switching at much higher frequencies and light load circumstances. The multiple-input soft-switching Cuk converter's closed-loop control technology will be the subject of future research.

REFERENCES

[1] B. P. Divakar and A. Ioinovici, "PWM converter with low stresses and zero capacitive turn-on losses," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 33, no. 3, pp. 913–920, Jul. 1997, doi: 10.1109/7.599311.

[2] R.-J. Wai, R.-Y. Duan, J.-D. Lee, and L.-W. Liu, "High-efficiency fuel-cell power inverter with soft-switching resonant technique," *IEEE Transactions on Energy Conversion*, vol. 20, no. 2, pp. 485–492, Jun. 2005, doi: 10.1109/TEC.2004.832092.

[3] S. Surya and V. Patil, "Cuk converter as an efficient driver for LED," in *2019 4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT)*, Dec. 2019, pp. 49–52, doi: 10.1109/ICEECCOT46775.2019.9114648.

[4] Z. Sun and S. Bae, "Multiple-input soft-switching Ćuk converter," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, pp. 2272–2276, doi: 10.1109/ECCE.2017.8096442.

[5] C.-J. Tseng and C.-L. Chen, "Zero-voltage-transition topologies for Cuk converters," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, vol. 2, pp. 930–935, doi: 10.1109/PESC.1998.703114.

[6] B. P. Divakar, K. W. E. Cheng, and D. Sutanto, "Zero-voltage and zero-current switching buck-boost converter with low voltage and current stresses," *IET Power Electronics*, vol. 1, no. 3, pp. 297–304, 2008, doi: 10.1049/iet-pel:20070038.

[7] T. Song and N. Huang, "A novel zero-voltage and zero-current-switching full-bridge PWM converter," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 286–291, Mar. 2005, doi: 10.1109/TPEL.2004.843016.

[8] N. S. Ting, I. Aksoy, and Y. Sahin, "A new zero-voltage-ransitiont PWM DC-DC boost converter," in *2015 Intl Aegean Conference on Electrical Machines & Power Electronics (ACEMP), 2015 Intl Conference on Optimization of Electrical & Electronic Equipment (OPTIM) & 2015 Intl Symposium on Advanced Electromechanical Motion Systems (ELECTROMOTION)*, Sep. 2015, pp. 257–262, doi: 10.1109/OPTIM.2015.7427027.

[9] H. Mao, F. C. Y. Lee, X. Zhou, H. Dai, M. Cosan, and D. Boroyevich, "Improved zero-current transition converters for high-power applications," *IEEE Transactions on Industry Applications*, vol. 33, no. 5, pp. 1220–1232, 1997, doi: 10.1109/28.633800.

[10] H. Bodur and A. F. Bakan, "An improved ZCT-PWM DC–DC converter for high-power and frequency applications," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 1, pp. 89–95, Feb. 2004, doi: 10.1109/TIE.2003.822091.

[11] Y. Zheng, B. Brown, W. Xie, S. Li, and K. Smedley, "High step-up DC–DC converter with zero voltage switching and low input current ripple," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9416–9429, Sep. 2020, doi: 10.1109/TPEL.2020.2968613.

[12] V. J. Samuel, G. Keerthi, and P. Mahalingam, "Coupled inductor-based DC–DC converter with high voltage conversion ratio and smooth input current," *IET Power Electronics*, vol. 13, no. 4, pp. 733–743, Mar. 2020, doi: 10.1049/iet-pel.2019.0933.

[13] H. G. Sadighi, S. E. Afjei, and A. Salemnia, "High step-up DC–DC converter based on coupled-inductor for renewable energy systems," *IET Power Electronics*, vol. 13, no. 18, pp. 4315–4324, Dec. 2020, doi: 10.1049/iet-pel.2020.0310.

[14] X. Zhang *et al.*, "Novel high step-up soft-switching DC–DC converter based on switched capacitor and coupled inductor," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9471–9481, Sep. 2020, doi: 10.1109/TPEL.2020.2972583.

[15] M. Vinduja, A. T. Surendran, and M. N. Madhu, "A high step-up DC-DC converter based on integrated coupled inductor and switched capacitor," in *2018 International Conference on Power, Signals, Control and Computation (EPSCICON)*, Jan. 2018, pp. 1–5, doi: 10.1109/EPSCICON.2018.8379609.

[16] P. Upadhyay, R. Kumar, and S. Sathyan, "Coupled-inductor-based high-gain converter utilising magnetising inductance to

achieve soft-switching with low voltage stress on devices," *IET Power Electronics*, vol. 13, no. 3, pp. 576–591, Feb. 2020, doi: 10.1049/iet-pel.2018.6147.
[17] M. E. Azizkandi, F. Sedaghati, H. Shayeghi, and F. Blaabjerg, "A high voltage gain DC–DC converter based on three winding coupled inductor and voltage multiplier cell," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4558–4567, May 2020, doi: 10.1109/TPEL.2019.2944518.
[18] L. Schmitz, D. C. Martins, and R. F. Coelho, "Comprehensive conception of high step-up DC–DC converters with coupled inductor and voltage multipliers techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 6, pp. 2140–2151, Jun. 2020, doi: 10.1109/TCSI.2020.2973154.
[19] S. H. Hosseini, T. Jalilzadeh, N. Rostami, and M. Maalandish, "A new topology for high step-up DC-DC converters," in *2017 10th International Conference on Electrical and Electronics Engineering (ELECO)*, 2017, pp. 259–263.
[20] P. Alavi, P. Mohseni, E. Babaei, and V. Marzang, "An ultra-high step-up DC–DC converter with extendable voltage gain and soft-switching capability," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 11, pp. 9238–9250, Nov. 2020, doi: 10.1109/TIE.2019.2952821.
[21] P. Mohseni, S. H. Hosseini, and M. Maalandish, "A new soft switching DC–DC converter with high voltage gain capability," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 9, pp. 7386–7398, Sep. 2020, doi: 10.1109/TIE.2019.2941130.
[22] L. Schmitz, D. C. Martins, and R. F. Coelho, "High step-up nonisolated ZVS/ZCS DC–DC converter for photovoltaic thin-film module applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 565–575, Mar. 2019, doi: 10.1109/JESTPE.2018.2830650.
[23] S. Sathyan, H. M. Suryawanshi, B. Singh, C. Chakraborty, V. Verma, and M. S. Ballal, "ZVS–ZCS high voltage gain integrated boost converter for DC microgrid," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 6898–6908, Nov. 2016, doi: 10.1109/TIE.2016.2582460.
[24] P. Mohseni, S. H. Hosseini, M. Maalandish, and M. Sabahi, "Ultra-high step-up two-input DC–DC converter with lower switching losses," *IET Power Electronics*, vol. 12, no. 9, pp. 2201–2213, Aug. 2019, doi: 10.1049/iet-pel.2018.5924.
[25] S.-W. Lee and H.-L. Do, "High step-up coupled-inductor cascade boost DC–DC converter with lossless passive snubber," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7753–7761, Oct. 2018, doi: 10.1109/TIE.2018.2803731.
[26] B. Arbetter, R. Erickson, and D. Maksimovic, "DC-DC converter design for battery-operated systems," in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, vol. 1, pp. 103–109, doi: 10.1109/PESC.1995.474799.

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