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Performance analysis of CMOS based analog circuit design with PVR variation

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ABSTRACT

Process, supply voltage, and temperature (PVT) are three important factors which contribute to performance variation of the complementary metal–oxide–semiconductor (CMOS) based analog circuits. In this paper, CMOS based analog circuit design with the PVT variation effects are explored. The effects of the PVT variation on the performance of CMOS based analog circuits are introduced. The optimization of CMOS based analog circuits such as differential amplifier (DA) and two-stage operational amplifier (op amp) circuits with PVT variations with different algorithms such as cockoo search (CS), particle swam optimization (PSO), hybrid CSPSO, and differential evaluation (DE) algorithms is presented. Each algorithm is implemented using the C programming language, interfaced with Ngspice circuit simulator, and tested on the Intel®core™ i5, 2.40 GHz processor with 8 GB internal RAM using the Ubuntu operating system (OS). The result shows PVT variation affects the performance of CMOS circuit.

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1. INTRODUCTION

The three important factors which contribute to performance variation of the complementary metal–oxide–semiconductor (CMOS) based analog circuits are process, voltage, and temperature (PVT) variations. The deviation in a fabrication creates process variations. The parameters which can create process variations can be impurity concentration densities, oxide thicknesses, and diffusion depths. This introduces variations in the sheet resistance and transistor parameters such as threshold voltage. This causes variations in (W/L) of MOS transistors. There are generally five possible process corners. They are known as typical-typical (TT), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF). The second parameter is the power supply on which MOS transistor performance depends. The variation in the supply voltage affects the saturation current which inflects the propagation delay of a cell. The supply voltage is not constant throughout the chip, hence the prorogation delay varies in a chip. Third factor is temperature variation that is unavoidable in the everyday operation of a design. The temperature can vary throghout the chip during chip operation. This happens due to the power dissipation in the MOS transistors. The power consumption is generally due to switching, short-circuit and leakage power consumption.

2. CIRCUIT DESIGN WITH PVT CORNERS

Cockoo search (CS) [1], [2], particle swam optimization (PSO) [3]–[5], differential evaluation (DE) [6], [7], and hybrid CSPSO [8] algorithms are tested for optimization of CMOS based analog circuits with

fixed PVT in different literature [9], [10]. By individually varying PVT factors over their permissible ranges, PVT variations can be taken into account. Analyzing subsequent combinations of above parameters are called PVT corners. In modern designs, there can be hundreds or thousands of PVT corners are posssible. The major intend of PVT analysis is to find the worst-case performance values across user-defined PVT corners. The strength and yield of the designed circuit are increased by guaranteeing that it complies with all design goals and constraints in some/all corners. The problem is that simulating each corner can take several seconds or minutes based on the complexity of the circuit. To simulate all possible corners could take hours or even days. Here, we have considered three process corners i.e TT, FF, and SS, three values of a supply voltage, and three values of temperature during PVT aware circuit design as a proof of concept. So, there would be a total of 3×3×3=27 combinations of the PVT corners. Two-step approach, as shown in Figure 1, is used to find the worst case performance with PVT analysis [8]–[11]. Different algorithm is discussed in defferenr literatures [12]–[23].

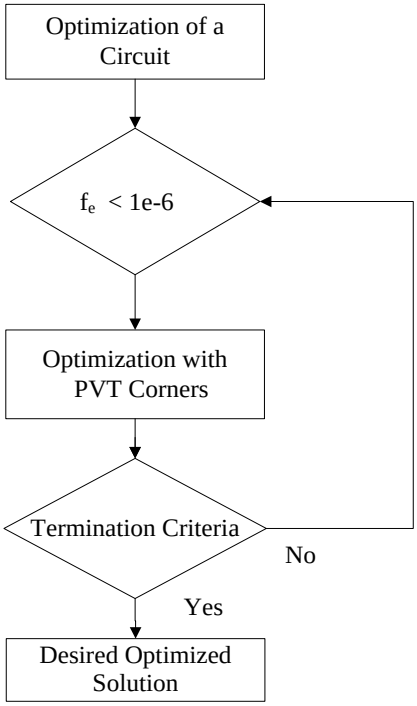

Figure 1. Two-step approach for circuit design with PVT variations [8], [11]

PVT corners are used within iterative circuit optimization loop for PVT-aware circuit optimization. After circuit optimization with the required fitness function value by the optimizer which is implemented using an evolutionary algorithms (EA), the circuit is tested with user-defined PVT corners. If the circuit gives required fitness value for each user-defined PVT corners then the optimization process will stop. If the circuit does not give required fitness value for any user-defined PVT corners then the optimizer will redesign the circuit until the termination criteria are not fulfilled. The termination criteria are the maximum number of iterations that have been reached or minimum fitness function value is satisfied. This process will stop when the termination criteria will meet.

3. OPTIMIZATION OF ANALOG CIRCUITS

The PVT analysis is carried out for differential amplifier (DA) and two-stage operational amplifier (op-amp) circuits using 0.18 µm CMOS technology during the optimization process with the CS, hybrid CSPSO, PSO, and DE algorithms.

3.1. Optimization of DA

The circuit diagram of DA is shown in Figure 2 [24], [25]. We have set a length of M1 to M4 transistors of DA circuit as $L_1=L_2=L_3=L_4=3.5$ µm, a length of M_5 and M_6 transistors as $L_5=L_6=1.4$ µm. The

circuit is optimized to drive the load capacitor of 0.5 pF. The supply voltage is set to ±1.8 V. Design parameters and search space of design parameters for DA using 0.18 µm CMOS technology are listed in Table 1. Desired specifications for this circuit using 0.18 µm CMOS technology are listed in Table 2.

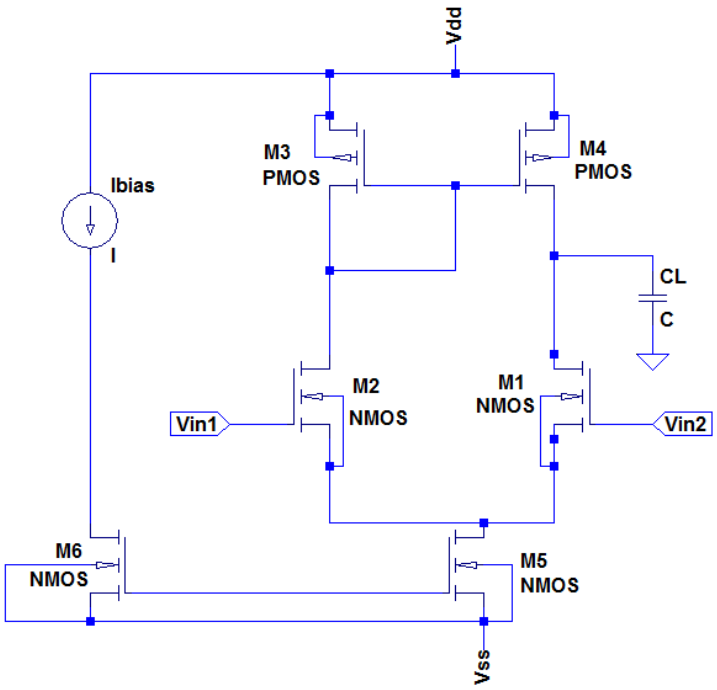

Figure 2. DA using a current mirror load [25]

Table 1. Design parameter and search space for DA using 0.18 µm CMOS technology

Sr. No.	Design parameters	Search space of design parameters
1	W_1=W_2 (µm)	3.5 µm to 30 µm
2	W_3=W_4 (µm)	3.5 µm to 30 µm
3	W_5=W_6 (µm)	3.5 µm to 30 µm
4	I_{bias} (µA)	3.5 µA to 30 µA

Table 2. Desired specifications for DA using 0.18 µm CMOS technology

Sr. No.	Specifications	Desired value
1	A_V (dB)	>39
2	UGB (MHz)	> 10
3	PM (°)	> 45
4	+ve PSSR (dB)	>35
5	- ve PSSR (dB)	>60
6	RSR (V/µs)	>9
7	FSR (V/µs)	>9
8	CMRR (dB)	>50
9	P_{diss} (mw)	< 1
10	N_{in} (nV^2/Hz)	< 1e-6
11	N_{op} (nV^2/Hz)	< 1e-4
12	TTA (μm^2)	< 1500

3.2. Optimization of two-stage OP-AMP

We have also optimized two-stage op-amp circuit using 0.18 µm CMOS technology at different PVT corners by the CS, hybrid CSPSO, PSO, and DE algorithms. The circuit diagram of the two-stage op-amp is given in the Figure 3 [24], [25]. We have set a length of M_1, M_2, M_5, M_7, and M_8 transistors as L_1=L_2=L_5=L_7=L_8=0.75 µm and a length of M_3, M_4, and M_6 transistors as L_3=L_4=L_6=0.50 µm for the optimization process with PVT corners using 0.18 µm CMOS technology. Design parameters and search space of design parameters for this circuit using 0.18 µm CMOS technology are listed in Table 3. Desired specifications for this circuit using 0.18 µm CMOS technology with are listed in Table 4.

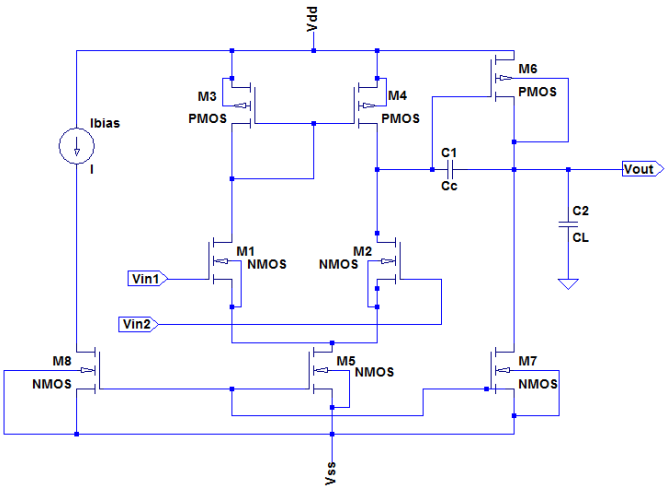

Figure 3. Two-stage op-amp [12], [13]

Table 3. Design parameters and search space for op-amp using 0.18 µm CMOS technology

Sr. No.	Design parameters	Search space of design parameters
1	W_1=W_2 (µm)	1 µm to 10 µm
2	W_3=W_4 (µm)	1 µm to 10 µm
3	W_5=W_8 (µm)	1 µm to 10 µm
4	W_6 (µm)	1 µm to 10 µm
5	W_7 (µm)	1 µm to 10 µm
6	I_{bias} (µA)	1 µA to 10 µA

Table 4. Desired specifications for op-amp using 0.18 µm CMOS technology

Sr. No.	Specifications	Desired value
1	A_V (dB)	> 60
2	UGB (MHz)	> 10
3	PM (°)	> 45
4	+ve PSSR (dB)	> 70
5	- ve PSSR (dB)	> 70
6	RSR (V/µs)	> 10
7	FSR (V/µs)	> 10
8	CMRR (dB)	> 60
9	P_{diss} (mw)	< 1
10	N_{in} (nV^2/Hz)	< 1e-6
11	N_{op} (nV^2/Hz)	< 1e-4
12	TTA (μm^2)	< 300

4. RESULTS AND DISCUSSION

Design parameters optimized by different EAs for DA using 0.18 µm CMOS technology at different PVT corners are listed in Table 5. Obtained specifications by different EAs for this circuit using 0.18 µm CMOS technology at different PVT corners are listed in Table 6. The CS and CSPSO algorithms optimized this circuit for the desired specifications with transport-triggered architecture (TTA) of 206.36 μm^2 and 195.85 μm^2 respectively. The TTA obtained by the CS and CSPSO algorithms is less as compared to that achieved by the DE and PSO algorithms. The performance of the CS, hybrid CSPSO, PSO, and DE algorithms for optimization of this circuit using 0.18 µm CMOS technology with PVT variations for 10 independent runs is listed in Table 7.

Table 5. Design parameters optimized by different EAs for DA using 0.18 µm CMOS technology at different PVT corners

Sr. No.	Design parameters	PSO	DE	CS	CSPSO
1	W_1=W_2 (µm)	24.10	28.63	17.75	17.22
2	W_3=W_4 (µm)	20.19	13.88	9.03	3.50
3	W_5=W_6 (µm)	26.03	23.77	24.79	18.14
4	I_{bias} (µA)	5.29	14.72	10.00	10.00

Table 6. Obtained specifications by different EAs for DA using 0.18 µm CMOS technology at different PVT corners

Sr. No.	Specifications	PSO	DE	CS	CSPSO
1	A_V (dB)	38.97	39.04	39.36	39.35
2	UGB (MHz)	14.00	25.68	25.17	21.70
3	PM (°)	49.83	45.44	51.60	53.50
4	+ve PSSR (dB)	40.48	40.99	40.86	41.36
5	- ve PSSR (dB)	72.52	72.54	71.59	68.51
6	RSR (V/µs)	14.68	33.47	27.16	23.66
7	FSR (V/µs)	9.96	23.12	19.55	18.62
8	CMRR (dB)	58.33	55.67	58.60	56.10
9	P_{diss} (mw)	0.03	0.07	0.05	0.05
10	N_{in} (nV^2/Hz)	2.66e-07	1.51e-07	1.27e-07	1.53e-07
11	N_{op} (nV^2/Hz)	1.91e-06	2.17e-06	1.64e-06	1.82e-06
12	TTA (μm^2)	382.95	364.08	256.86	195.85

Table 7. Performance of different EAs for optimization of DA using 0.18 µm CMOS technology with PVT variations

Algorithm	$SD_{fitness}$	I_{avg}	FE_{avg}	S_{rate}	T_{sim} (s)
DE	0.001403	36.10	1113	9	2511
PSO	0.002032	60.4	1812	4	4428
CS	0.004117	17.4	1074	9	2488
CSPSO	0.0	30.9	2811	10	5594

The CSPSO algorithm succeeded 10 times, the CS and DE algorithms succeeded 9 times, and the PSO algorithm succeeded only 1 time out of 10 runs to achieve all specifications. The CS algorithm required less average iterations for 10 independent runs of the optimization process compared to those required for DE and PSO algorithms. The CSPSO algorithm also achieved zero standard deviation of fitness value. Thus, the performance of the CS and CSPSO algorithms outperform compared to DE and PSO algorithms for this case.

The convergence graph of CS, CSPSO, DE, and PSO algorithms for the optimization of DA using 0.18 µm CMOS technology at different PVT corners is shown in Figure 4 which shows that the CS algorithm is faster to reach at target fitness value as compared to DE, CSPSO, and PSO algorithms. Design parameters optimized by different EAs for this circuit using 0.18 µm CMOS technology with PVT variations are listed in Table 8. Obtained specifications by different EAs for this circuit using 0.18 µm CMOS technology with PVT variations are listed in Table 9.

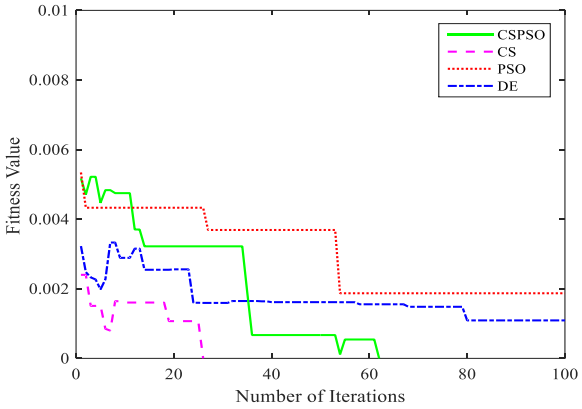

Figure 4. Convergence graph of different EAs for DA optimization using 0.18 µm CMOS technology at different PVT corners

Table 8. Design parameters optimized by different EAs for Op-amp using 0.18 µm CMOS technology at different PVT corners

Sr. No.	Design parameters	PSO	DE	CS	CSPSO
1	W_1=W_2 (µm)	9.50	10.00	1.70	1.52
2	W_3=W_4 (µm)	7.12	6.81	3.32	3.90
3	W_5=W_8 (µm)	9.02	10.00	3.55	5.38
4	W_6 (µm)	9.78	9.67	8.53	10.00
5	W_7 (µm)	10.00	10.00	5.85	7.15
6	I_{bias} (µA)	9.04	10.00	9.95	9.13

Table 9. Obtained specifications by different EAs for Op-amp using 0.18 µm CMOS technology at different PVT corners

Sr. No.	Specifications	PSO	DE	CS	CSPSO
1	A_V (dB)	66.42	66.54	68.38	68.84
2	UGB (MHz)	25.55	21.51	11.81	10.83
3	PM (°)	27.90	106.20	45.19	48.71
4	+ve PSSR (dB)	81.66	80.94	80.65	81.46
5	- ve PSSR (dB)	90.06	91.62	90.75	109.84
6	RSR (V/µs)	15.69	15.07	15.42	15.11
7	FSR (V/µs)	10.89	9.95	13.70	12.25
8	CMRR (dB)	73.94	73.11	72.97	71.69
9	P_{diss} (mw)	0.07	0.07	0.11	0.10
10	N_{in} (nV^2/Hz)	8.54e-08	1.37 e-07	3.51e-07	4.02 e-07
11	N_{op} (nV^2/Hz)	2.40e-05	3.02 e-05	4.14e-05	4.65e-05
12	TTA (μm^2)	47.29	46.43	19.85	24.61

The CS algorithm optimized this circuit with least TTA of 19.85 μm^2 as compared to that achieved by other algorithms. The performance of the CS, PSO, hybrid CSPSO, and DE algorithms for optimization of this circuitusing 0.18 µm CMOS technology for 10 independent runs is listed in Table 10. The CSPSO algorithm succeeded 6 times, the CS succeeded 3 times, and the DE algorithm succeeded only 1 time out of 10 runs to achieve all specifications, whereas the PSO algorithm did not succeed to achieve all specifications. The CSPSO and CS algorithms required less average iterations for 10 independent runs of the optimization process of this circuit compared to those required for DE and PSO algorithms. Thus, the performance of the CSPSO and CS algorithms outperforms compared to both DE and PSO algorithms for this case also. The convergence graph of CS, CSPSO, DE, and PSO algorithms for the optimization of two-stage op-amp using 0.18 µm CMOS technology is shown in Figure 5 which shows that the CSPSO algorithm is faster to reach at target fitness value as compared to DE, CS, and PSO algorithms.

Table 10. Performance of different EAs for optimization of op-amp using 0.18 µm CMOS technology with PVT variations

Algorithm	$SD_{fintess}$	I_{avg}	FE_{avg}	S_{rate}	T_{sim} (s)
DE	0.378508	90.4	3,030	1	4879
PSO	0.269239	100	3,000	0	4765
CS	0.106352	85.30	5,148	3	8140
CSPSO	0.282675	66	5,970	6	9651

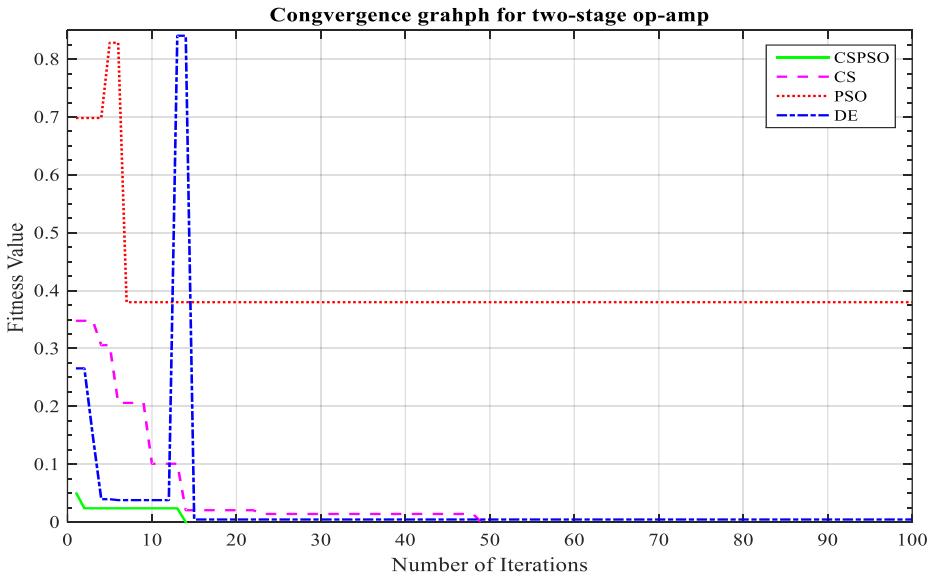

Figure 5. Convergence graph of different EAs for two-stage op-amp optimization using 0.18 µm CMOS technology

5. CONCLUSION

In this paper, the focus is set on PVT-aware circuit optimization to find a design which meets desired specifications across all user-defined PVT corners. DA and two-stage op-amp circuits with different 27 PVT corners are optimized for required specifications using 0.18 µm CMOS technology by different metaheuristic EAs. The performance of each EA is also compared for PVT-aware design of DA and two-stage op-amp circuits. The CS and CSPSO algorithms outperform compared to both DE and PSO algorithms for PVT-aware circuit optimization. The PVT analysis is important to develop a robust optimizer.

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