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Design and implementation reversible multiplexer using quantum-dot cellular automata approach

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ABSTRACT

Rapid progress in the field of nanotechnology includes using quantum dot-cellular automata (QCA) as a replacement for conventional transistor-based complementary metal oxide semiconductor (CMOS) circuits in the construction of nano-circuits. Due to ultra low thermal dissipation, rapid clocking, and extremely high density, the QCA is a rapidly growing field in the nanotechnological field to inhibit the field effect transistor (FET)-based circuit. This paper discusses and evaluates two multiplexer (MUX) architectures: an innovative and effective 4×1 MUX structure and an 8×1 MUX structures using QCA technology. The suggested architectural designs are constructed using the Fredkin and controlled-NOT (CNOT) gates. These constructions were designed to simulate using tool QCA designer 2.0.3. The 591 and 1,615 cells would be used by the 4×1 and 8×1 QCA MUX architectures, respectively. The simulation results demonstrate that, when compared to the previous QCA MUX structures, the suggested QCA MUX designs have the best clock latency performance and use of different gate types.

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1. INTRODUCTION

Data loss is one of the confrontation problems in the development of prototypes and systems. Reversible counting is a probable solution to this problem by letting the counting be done at the logical scale without data loss by establishing the number of inputs equal to the number of outputs [1]. The main goal of implementing reversible circuits is to decrease the number of logic gates, garbage outputs, fixed inputs, and quantum costs. The quantum dot cellular automata (QCA) have emerged as a potential computational structure for the modernization of nano computing systems. It has a large ability in the growth of circuits with high space intensities and dispersion of low heat and permits faster computers to develop with lower power consumption. QCA is a new instrument to produce nano-level digital equipment, study and resolve their various parameters. It is also a potential technology for low power and high-intensity memory plans [2]. The advantages of QCA are i) lower power because there is no current outflow only energy required to add to raise the electrons from their ground situation [3], ii) quantum cells are very tiny scaled in nano-scale and demands less very less region [4].

The aim of this paper is to suggested QCA designs for reversible multiplexers (MUXs) using a fundamental building block. The fundamental building block can be requested to implement their required gate. It is possible to present the suggested implementation of the MUX to develop quantum gates including controlled-NOT (CNOT) and Fredkin gates (FG) because QCA designs will be utilized as building blocks. It is

possible to implement reversible circuits with many quantum gates using fundamental building block. The QCA designer tool, version 2.0.3, has been used to implement and simulate the QCA circuits in this paper.

2. METHOD

The QCA fundamentals and constructions are introduced first in this section. The reversible gates (Fredkin and CNOT) are then explained, followed by the MUX structure.

2.1. Fundamental quantum dot automata construction

On a nanoscale, QCA technology could replace field effect transistor (FET)-based devices [5]. Regards to elevation power consumption, finite physical density, and elevation current leakage, complementary metal oxide semiconductor (CMOS) is reaching the transistor finite point in operation [6]. By placing charges among quantum dots, QCA is a transistor-free processing technique that encodes binary information [7].

This method is cell-based. As illustrated in Figure 1, each cell has two electrons and four transporters that serve as storage for the electrons. Tunnels are used to carry these electrons from one transporter to another [8]. Figure 2 depicts a fourth quantum point QCA.

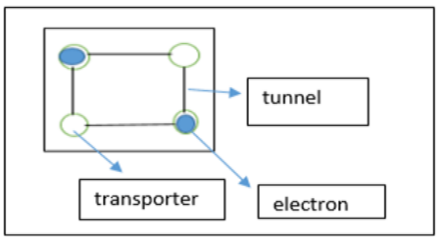


Figure 1. Cell of QCA

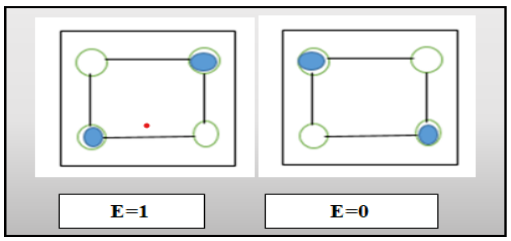


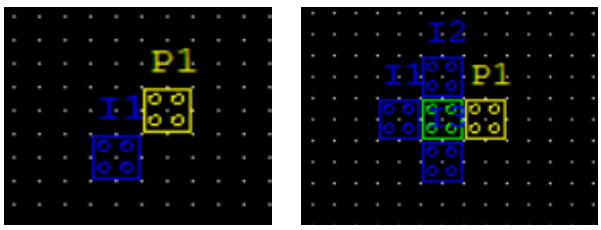
Figure 2. QCA cells with fourth quantum points (E=1(binary 1), E=0(binary 0)

These free electrons are forced to shift to the diagonally reversed locations by their columbic interaction. There are then only two conceivable states, depending on the placement of the electron. This results in two polarizations in the QCA cell [9]. The state polarizations are denoted by the numbers -1 for binary zero and +1 for binary one [10]. These polarizations in the 0 and 1 states can be expressed as in (1) [11].

$$E = \frac{(E1+E3)-(E3+E4)}{E1+E2+E3+E4} \quad (1)$$

Many QCA cells make up the QCA wires, which can be utilized to transmit input cell polarization. Two collections of QCA wire are possible: i) single-layer crossing wires; ii) multiple-layer crossing wires [12]. In QCA circuits, two wire types 90 degree and 45 degrees are used. The wire of basis cells that have been rotated by 45 degrees is known as the 45 degrees [13]. Inverter gate (NOT) and majority gate (MG) are the two main QCA gates [14], [15]. NOT gate and MG (majority gate) are represented in Figures 3(a) and 3(b). MG's neutralizing role is its logical purpose can be expressed as in (2).

$$F(I1, I2, I3) = I1I2 + I1I3 + I2I3 \quad (2)$$



(a) (b)

Figure 3. The primary QCA gates (a) NOT gate and (b) MG gate

2.2. Clock of QCA

QCA system contain the clocks that's supply power for automation and for control the flowing data. Cell of QCA has four phases: switch, hold, release, and relax. In case of switch, the cells start un-polarized and with low potential barriers but the barriers are raised during this case. In case of hold ,the barriers are held high [16] every cell fetches polarized after the electrons proceed to the dots which need the lowest energy depending on the driver cell [17] while the case of release, the barriers become low. In last case of relax, the barriers keep low and the cells remain in an un-polarized state [16]. Circuit of QCA can be splitted into 4 areas which each area comprises four phases stated in Figure 4 [17].

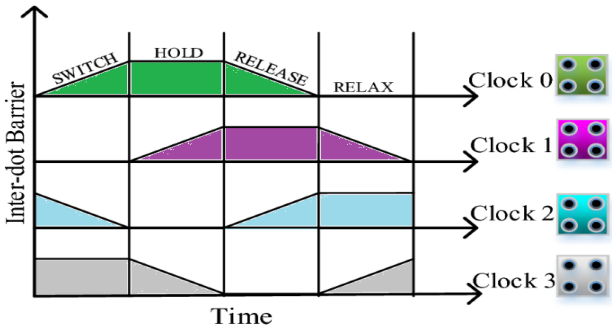


Figure 4. Clock signal of QCA

2.3. FG

FG contain three inputs (I_1, I_2, I_3) and three outputs (P_1, P_2, P_3) that swap the last two bits if the first bit is one. It is used as multiplexer (N*1MUX) and out of three inputs, one input used as enable where $P_1=I_1$, $P_2=I_1' I_2+I_1I_3$, and $P_3= I_3 I_1+ I_1' I_2$ [18]. it is also self-reversible as it is its own inverse. It is a prefecture gate because the number of logical ones (hamming weight) of an input is same as its output [19]. Figure 5 shows a block diagram of a Fredkin gate and Table 1 demonstrates its truth table.

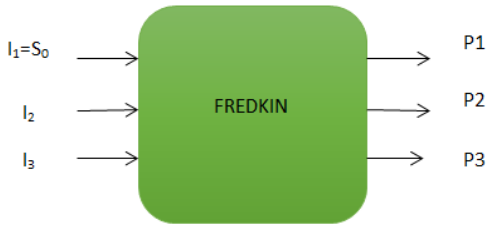


Figure 5. Fredkin gate

Table 1. Fredkin truth table

P_3	P_2	P_1	I_3	I_2	I_1
0	0	0	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	1	1	0
0	0	1	0	0	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	1	1	1	1
0	0	0	0	0	0

2.4. CNOT gate

CNOT (Feynman) gate is general used for sign copying or to get the supplement of the data flag. It is contain two inputs (I_1, I_2) and two outputs (P_1, P_2) where $P_1=I_1$ and $P_2=I_1$XOR I_2 [20], [21]. Figure 6 shows a block diagram of a CNOT gate and Table 2 demonstrates its truth table.

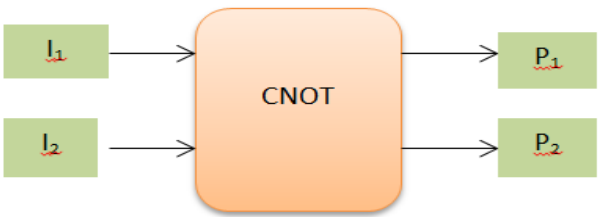


Figure 6. CNOT gate

Table 2. CNOT truth table

I_1	I_2	P_1	P_2
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2.5. MUX

A MUX is an essential piece of equipment in the modeling and simulation of digital memory circuits [22]. A combinational circuit really does have multiple inputs (one or more select inputs) but just one output. Signals are passed from one of the inputs to the output. Figure 7 [23], [24] show it. It receives binary information [0,1] from various input lines or sources and routes a specific input line to a single output line based on the set of select lines or sources. A reversible 2^b -to-1 MUX can be implemented using only a 2^b-1 gate, which generates 2^b+b-1 garbage outputs. It also requires a $5(2^b- 1)$ reversible cost and a $5(2^b- 1)$ Λ delay, where b corresponds to the number of selection lines and Λ defines the unit delay [25].

Figure 8 demonstrates a 2x1 MUX block diagram. It has two inputs, one selection, and one output. It is constructed by onereversible FG, with first input being selection (I_1) and the second output (P_2) being the MUX output. Figure 9 demonstrates a layout of a 2×1 MUX using QCA technique [26]. The following (3) [27] can be used to express the output (P_2) and the truth table for a 2×1 MUX can be seen in Table 3. Figure 10 illustrates the simulation result of the 2×1 MUX design using 75 cells with 0.18 μm^2.

$$P2 = S0'I2 + S0I3 \quad (3)$$

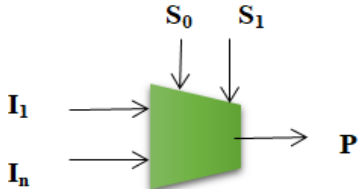


Figure 7. MUX model

Figure 8. 2×1 MUX

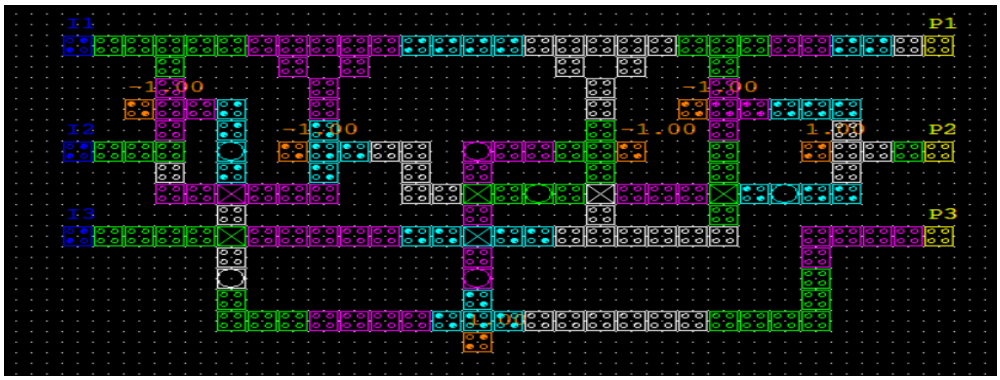


Figure 9. 2×1 MUX using Fredkin reversible gate

Table 3. 2×1 MAX (truth table)

$I_1(S_0)$	I_2	I_3	P_2
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

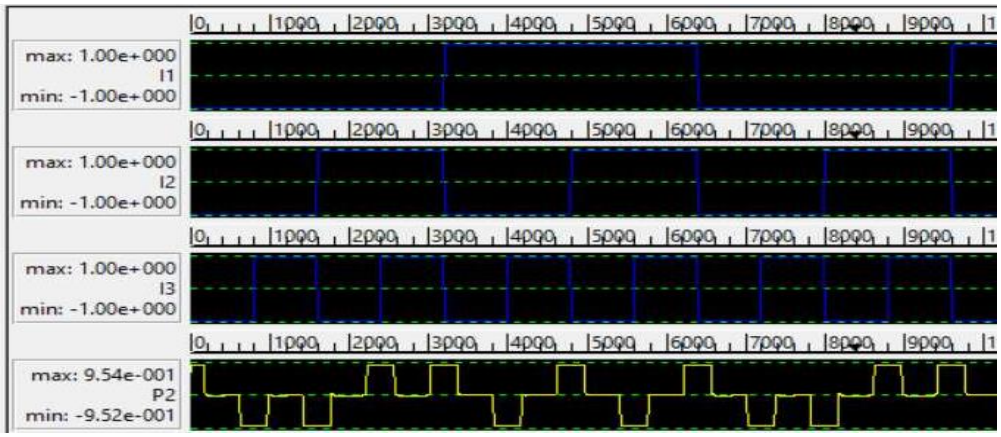


Figure 10. Simulation result of 2×1 MUX

3. PROPOSED MULTIPLEXER

This section is split into two parts: the first presents 4×1 MUX structures that use Fredkin, CNOT reversible gates, and the second part needs an implementation of a new 8×1 MUX using the unique structure suggested in the first part.

3.1. 4×1 MUX

The 4×1 MUX has four inputs, two selection paths, and one output. Figure 11 demonstrates a suggested 4×1 MUX block diagram. Three Fredkin gates (three 2×1 MUX) and two CNOT gates have been used. Figure 12 demonstrates the layout of a 4×1 MUX using the QCA technique.

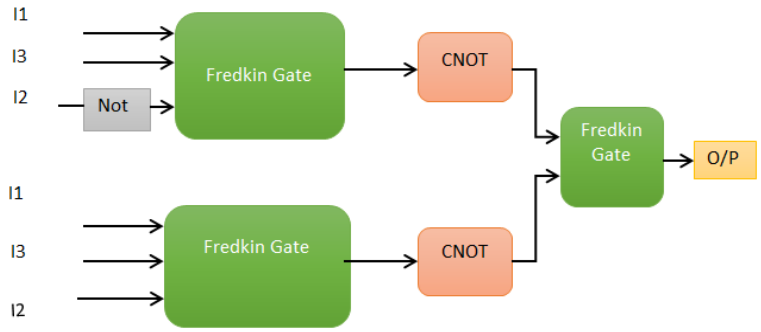


Figure 11. Suggested block diagram of 4×1 MUX

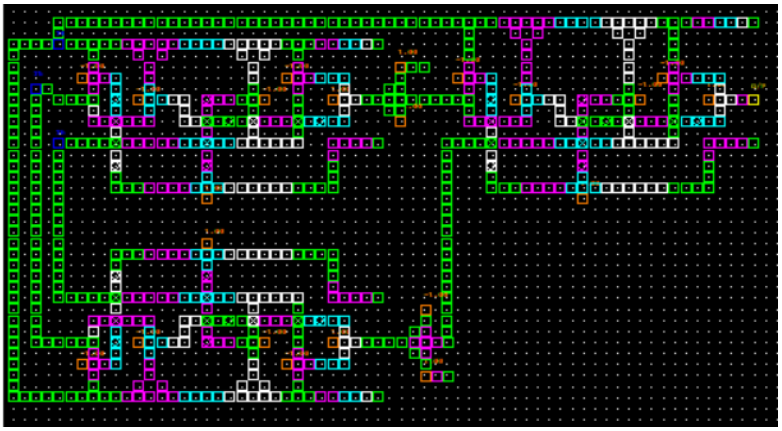


Figure 12. Structure of 4×1 MUX using QCA

3.2. 8×1 MUX

An 8-to-1 MUX must have eight data inputs, three input select lines, and a single output line. The MUX chooses the inputs based on the selected line combinations. Figure 13 demonstrates a suggested 8×1 MUX block diagram. Seven Fredkin gates (two 4×1 MUX and one 2×1 MUX) and six CNOT gates have been used. Figure 14 demonstrates the layout of an 8×1 MUX using the QCA technique.

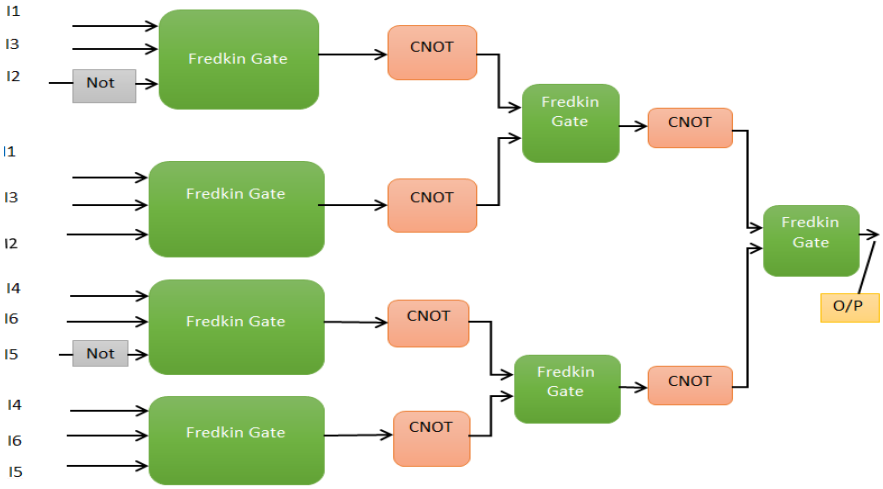


Figure 13. Suggested block diagram of 8×1 MUX

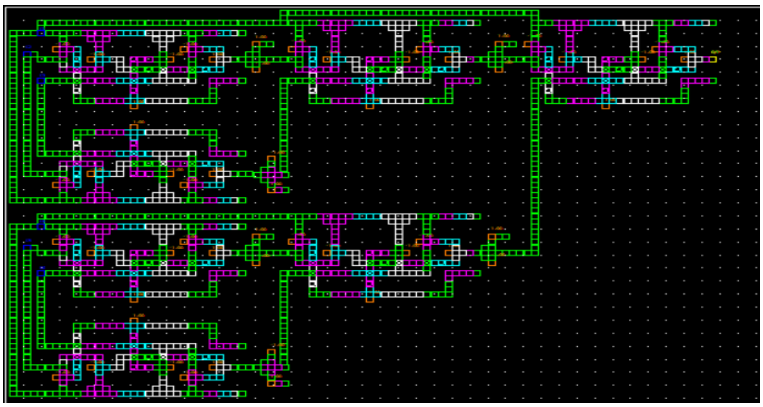


Figure 14. Structure of 8×1 MUX using QCA

4. SIMULATION AND RESULTS

QCA designer is a simulation software was using to evaluate QCA logic circuits. QCA simulation results are including bi-stable approximation and coherence vector. approximation bi-stable determine the state of a single cell in a time-independent manner using retinal energy neutralization, which determines the cost of two cells with flip polarization, lowering simulation time in this type. Each cell can be worked in 4 steps: input (blue cell), output (yellow cell), fixed (polarization cell), and normal (green cell) seen in Figure 15. The bistable approximation is used to provide input combinations with the parameters seen in the Table 4.

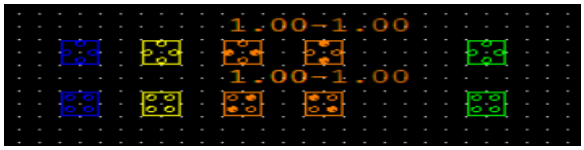


Figure 15. QCA design cells

Table 4. Bi-stable approximation parameters

Parameters	Value
Cell standard	18 nm
Numbering samples	12800
Radius of effect (nm)	65.000000
Clock	9.800000e-022(high), 3.800000e-023(low)
Factor of clock amplitude	2.000000
MAX iterations per samples	100.00
Layer separation	11.500000

The different designs that have previously been designed have been taken into account. Previous designs are compared to a suggested 4×1 and 8×1 MUX. Tables 5 and 6 make a comparison these designs to the suggested design through terms of the area, number of cells, response time, and number of gates used in constructed MUX. Figure 16 illustrates the simulation result of the suggested 4×1 MUX design using 591 cells with 0.93 μm^2. Figure 17 illustrates the simulation result of the suggested design of an 8×1 MUX using 1,615 cells with 2.95 μm^2.

Table 5. 4×1 MUX result comparison

4×1 MUX	Gate types used in design	Overall Area (μm^2)	The number of cells used	Response Timein terms clock zones
[5]	Magority+Inverter	0.14	104	1.75
[7]	Magority + Inverter	0.11	82	1+3/4
[8]	Magority+ Inverter	0.202	118	4
[10]	Magority	0.22	193	1.75
[12]	Magority +Inverter	0.11	96	1
[17]	Magority	0.03	37	3
[22]	Magority	0.06	49	3
[27]	Magority	0.04	-	5
Suggested	Fredkin +CNOT	0.93	591	1.5

Table 6. 8×1 MUX result comparison

8×1MUX	Gate types used in design	Overall Area (μm^2)	The number of cells used	Response Timein terms clock zones
[5]	Magority+Inverter	0.39	312	2.5
[12]	Magority +Inverter	0.43	286	1.5
[22]	Magority	0.20	156	6
Suggested	Fredkin +CNOT	2.95	1615	2

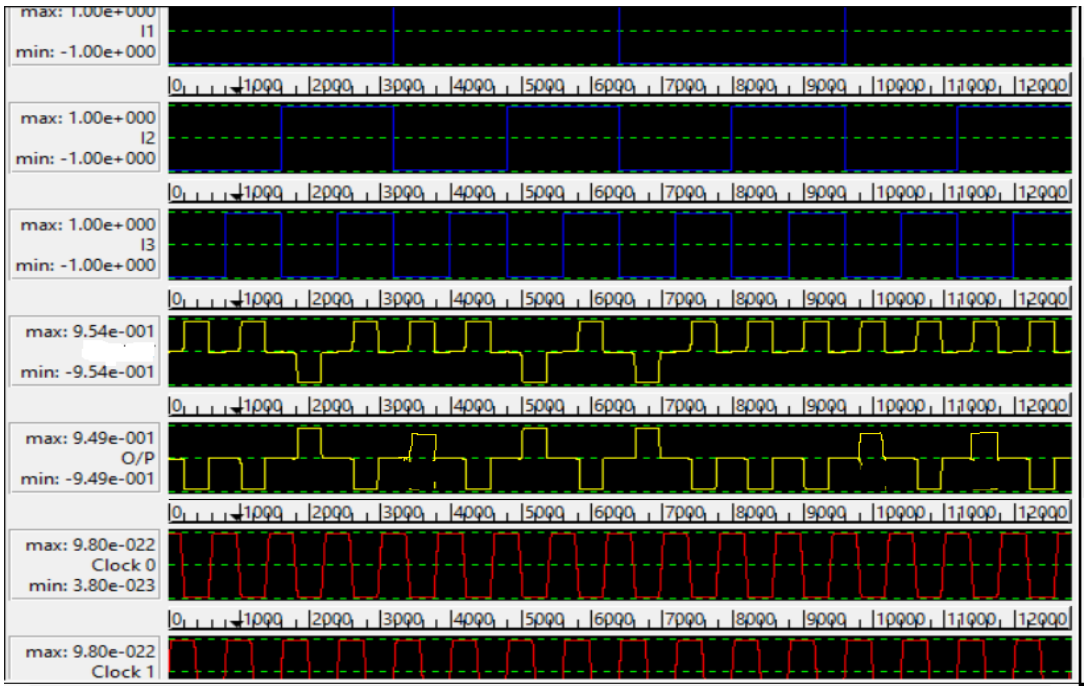


Figure 16. Simulation result of suggested 4×1 MUX

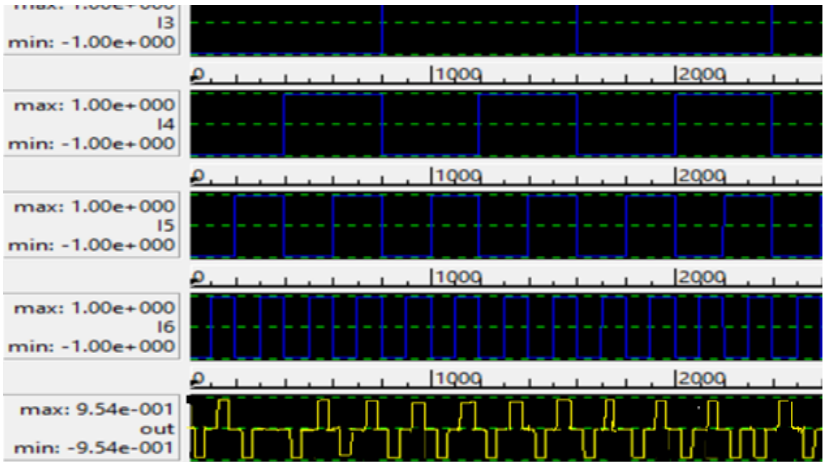


Figure 17. Simulation result of suggested 8×1 MUX

5. CONCLUSION

In this paper, we proposed an efficient multi-layer circuit for a 4×1 QCA MUX based on Fredkin and CNOT gates. This 4×1 QCA MUX circuit is then used to suggest 8×1 QCA MUX circuits. The suggested circuits for QCA MAX have been simulated using QCA designer 2.0.3. The suggested 4×1 and 8×1 MUX circuits used 591 (0.93 m^2) and 1615 (2.95 m^2) QCA cells in their overall area, according to the results. When compared with existing circuits, the results indicate that the suggested 4×1 and 8×1 MUX circuits improved response time in terms of clock zones and different gate types used in implementation.

REFERENCES

[1] A. Moustafa, A. Younes, and Y. F. Hassan, "A customizable quantum-dot cellular automata building block for the synthesis of classical and reversible circuits," *The Scientific World Journal*, vol. 2015, 2015, doi: 10.1155/2015/705056.

[2] S. A. and N. J. Navimipour, "Memory designing using quantum-dot cellular automata: systematic literature review, classification and current trends," *Journal of Circuits, Systems and Computers*, vol. 26, no. 12, p. 1730004, 2017, doi/10.1142/S0218126617300045.

[3] D. Mukhopadhyay, "Designing and implementation of quantum cellular automata 2 : 1 multiplexer circuit," *International Journal of Computer Applications*, vol. 25, no. 1, pp. 21–24, Jul. 2011.

[4] G. M. Shanthala and P. Karthik, "Design and implementation of scan flip-flop for processor using QCA technology," *International journal of control and automation*, vol. 10, no. 8, pp. 41–52, 2017.

[5] M. Kianpour and R. Sabbaghi-Nadooshan, "Optimized design of multiplexor by quantum-dot cellular automata," *International Journal of Nanoscience and Nanotechnology*, vol. 9, no. 1, pp. 15–24, 2013.

[6] N. Safoev, "An optimal design of multiplexer based conservative gate in quantum-dot cellular automata," *ICWMC*, vol. 108, pp. 100–101, 2017.

[7] A. M. Chabi, S. Sayedsalehi, S. Angizi, and K. Navi, "Efficient QCA exclusive-or and multiplexer circuits based on a nanoelectronic-compatible designing approach," *International scholarly research notices*, vol. 2014, pp. 1–9, 2014, doi: 10.1155/2014/463967.

[8] A. Tambe, S. Bhakre, and S. Kassa, "Design and analysis of (2×1) and (4×1) multiplexer circuit in quantum dot cellular automata approach," *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, vol. 8, no. 6S3, pp. 277–281, Apr. 2019.

[9] A. Rezaei, "New efficient designs of reversible logic gates and circuits in the QCA technology," *Engineering Review*, vol. 39, no. 1, pp. 47–59, 2019, doi: 10.30765/er.39.1.6.

[10] A. Mallaiah, G. N. Swamy, and K. Padmapriya, "Designing efficient multiplexer, demultiplexer QCA logic circuits and power dissipation analysis –a new approach," vol. 9, no. 7, pp. 1995–2004, 2018.

[11] S. S. Kavitha and N. Kaulgud, "Quantum dot cellular automata (QCA) design for the realization of basic logic gates," *2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT)*, 2017, pp. 314–317, doi: 10.1109/ICEECCOT.2017.8284519.

[12] H. Rashidi and A. Rezai, "Design of novel multiplexer circuits in QCA nanocomputing," *Facta Universitatis. Series: Electronics and Energetics*, vol. 34, no. 1, pp. 105–114, 2021, doi: 10.2298/fuee2101105r.

[13] Y. Rahmani, S. R. Heikalabad, and M. Mosleh, "Design of a new multiplexer structure based on a new fault-tolerant majority gate in quantum-dot cellular automata," *Optical and Quantum Electronics*, vol. 53, no. 9, pp. 1–23, 2021, doi: 10.1007/s11082-021-03179-1.

[14] M. Y. Nejad and M. Mosleh, "A review on QCA multiplexer designs," *Majlesi Journal of Electrical Engineering*, vol. 11, no. 2, pp. 69–79, 2017.

[15] S. Hashemi, M. R. Azghadi, and A. Zakerolhosseini, "A novel QCA multiplexer design," *2008 International Symposium on Telecommunications*, 2008, pp. 692–696, doi: 10.1109/ISTEL.2008.4651389.

[16] B. B. Pandey, N. Tiwari, and N. Ahmad, "Multiplexer design based on majority gate with quantum cellular automata," *National Conferences on Challenges & Opportunities for Technological Innovation*, 2013.

[17] E. AlKaldy, A. H. Majeed, M. S. bin Zainal, and D. B. M. D. Nor, "Optimum multiplexer design in quantum-dot cellular

automata," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 17, no. 1, pp. 148–155, Jan. 2020, doi: 10.11591/ijeecs.v17.i1.pp148-155.
[18] N. H. Sherif and M. H. Ali, "A review: asynchronous counters using quantum gates," *IOP Conference Series: Materials Science and Engineering*, vol. 928, no. 2, p. 022031, Nov. 2020,doi:10.1088/1757-899X/928/2/022031.
[19] B. Ravichandra and R. Kumar Aswamy, "FPGA implementation of basic adder circuits using reversible logic gates," pp. 81–89.
[20] S. Syed, N. M. Huq, and S. M. Das, "Implementation of reversible combinational multiplxers using reversable gates," *Journal of Engineering Sciences*, vol. 10, no. 12, pp. 264–274, 2019, doi: 10.15433.JES.2019.V10I12.43P.42.
[21] E. J. Alex and A. P. Kumar, "Fredkin gates based testable reversible shift registers," *International Journal of Innovative Technology and Exploring Engineering*, vol. 8, no. 11, pp. 154–163, Sep. 2019, doi: 10.35940/ijitee.K1025.09811S219.
[22] A. Hariprasad and S. K. Chennupati, "Qunatum-dot cellular automata technology based optimized multiplexers design," *International Journal of Recent Technology and Engineering (IJRTE)*, vol. 8, no. 2, pp. 2717–2725, Sep. 2019, doi: 10.35940/ijrte.B1333.0982S1119.
[23] J. C. Das and D. D. De, "Optimized multiplexer design and simulation using quantum dot-cellular automata," *Indian Journal of Pure & Applied Physic (IJPAP)*, vol. 54, no. 12, pp. 802–811, Dec. 2016.
[24] V. Mardiris, C. Mizas, L. Fragidis, and V. Chatzis, "Design and simulation of a QCA 2 to 1 multiplexer," *12th WSEAS International conference on computers, Heraklion*, pp. 572–576, Jul. 2008.
[25] H. M. H. Babu, "Quantum computing A pathway to quantum logic design," *IOP ebooks*, 2020, doi: 10.1088/978-0-7503-2747-3.
[26] P. Biswas, N. Gupta, and N. Patidar, "Basic reversible logic gates and it's QCA implementation," *Journal of Engineering Research and Applications*, vol. 4, no. 6, pp. 12–16, Jun. 2014.
[27] A. Almatrood and A. K. George, "Low-power multiplexer structures targeting efficient QCA nanotechnology circuit designs," *Electronics*, vol. 10, no. 16, p. 1885, Aug. 2021, doi: 10.3390/electronics10161885.

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