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A cascade multi-level inverter topology with reduced switches and higher efficiency

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ABSTRACT

The use of multi-level inverter (MLI) technologies in high-power, medium-voltage energy regulation has been more popular in recent years. Despite the fact that the multilayer inverter has a lot of benefits, it has certain disadvantages in the layer of higher levels due to the enormous number of semiconductor switches that it employs in its construction. This may result in the inverter being of a huge size and costing a lot of money, as well as a significant rise in losses. As a result, the new MLI is suggested to minimize the number of switches in order to alleviate these challenges. This article describes a cascaded multilevel inverter with lower devices. The suggested cascaded multilevel inverter is intended for use in minimizing total harmonic distortion (THD), as shown in MATLAB/Simulink by the graph. Multilevel inverters benefit from the switching pattern of semiconductor switches, which may be used to improve their overall performance. This approach lowers the switching loss while simultaneously increasing the efficiency. In order to validate the suggested approach, simulations are carried out using the MATLAB/Simulink programming environment.

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1. INTRODUCTION

In recent years, there has been a lot of interest in multi-level inverters (MLIs) because of their potential uses in industrial and electrical systems, as well as their minimal electromagnetic interference, ease of control, and high efficiency. Additionally, it is possible to link it up to various renewable energy sources such as wind turbines, and photovoltaic solar panels [1]-[8]. Since 1970, various topologies have been developed [9]. The two-level inverter is the most common type of inverter, and it is named for the fact that it produces two different voltage levels. However, the performance of this inverter is affected by a high level of total harmonic distortion (THD), leading to the need of a large filter size, a high voltage rating for the switches, a high switching frequency, which results in additional switching losses, increased voltage stress on the switches, and electromagnetic interference. The two-level inverter can only be utilized for applications that involve low and medium voltage [10]-[15]. This is because the switches have a high voltage rating and are subject to voltage stress. This brings up the requirement for a different configuration. MLI is presented in order to provide a DC/AC conversion that has significantly improved performance and significantly reduced THD [16]-[18].

The best operation of most electrical applications is ensured by using a sinusoidal waveform supply [19]-[21]. With an increase in the number of inverter levels, the output voltage becomes more similar to a sinusoidal waveform, hence lowering the THD [22], [23]. When compared to the hard-switched two-level

pulse width modulation (PWM) inverter, the MLI has a number of advantages, including a lower dv/dt at high power operation and higher efficiency [24]-[26].

Generally, there are three main topologies for MLIs: cascade, diode clamp, and capacitor clamp. Among these topologies are the following: the cascade MLI is the simplest to construct and has the fewest number of components [24], [27]. Typically, cascade MLI is made up of a number of switches and DC sources that are all connected in series. To generate alternating current voltage with several levels, the switches must be toggled on and off in order to achieve the fundamental voltage and eliminate the higher order harmonics in the output. In this paper, a cascade of MLIs is presented and compared with three inverter topologies to get the fewest number of switches possible to reduce the size and cost of the converter and to reduce switching losses by reducing the number of switches in the on-state during each mode of operation, which improves efficiency.

2. RESEARCH METHOD

2.1. Conventional cascade bridge MLI topology

Figure 1 depicts the conventional cascade bridge MLI topology that is commonly used [22]. The output voltage level of this inverter is:

$$k = (N + 2)/2 \quad (1)$$

where N represents the number of switches necessary to achieve the desired voltage level.

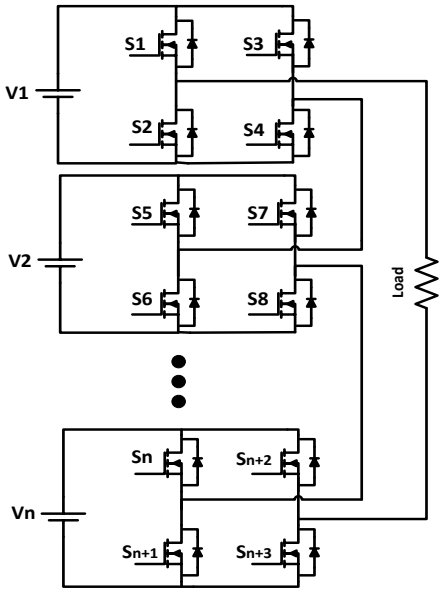

Figure 1. The conventional cascade bridge MLI

2.2. The cascade MLI topologies

The topology for the cascade MLI as a modified topology for the cascade bridge MLI as shown in Figure 2 [28]. As can be seen in Figure 2, the number of switches in the level marker part is 5, with three individual DC sources to form two cascade cells connected in series, in addition to the four switches in the H-bridge part. The number of output voltage levels depends upon the number of cells. The number of switches is reduced considerably compared to the conventional cascade bridge MLI for the same output voltage level. To reduce the THD in the output voltage the number of output voltage levels must be increased but this will require more DC sources and switches and need more complex control circuit. The output voltage level of this inverter is:

$$k = N - 2 \quad (2)$$

$$N = 2n + 3 \quad (3)$$

Where N is number of switches and n is the number of DC sources.

The 7-level cascade MLI topology in [7] can be improved as shown in Figure 3. In this figure, one of the two switches in each cell is replaced by a diode. The required number of switches and diodes required can be calculated as:

$$\text{Number of switches } (N) = n + 4 \quad (4)$$

$$\text{The number of diodes} = (k-3)/2 \quad (5)$$

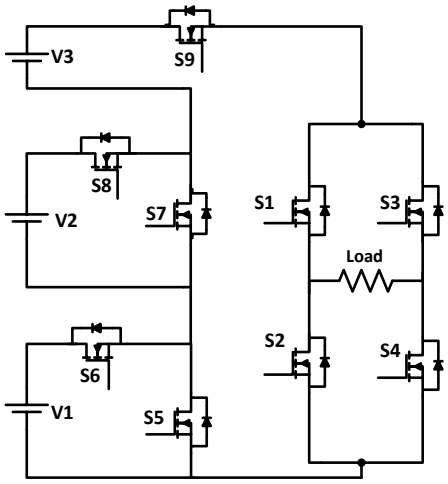

Figure 2. The cascade bridge 7-level inverter

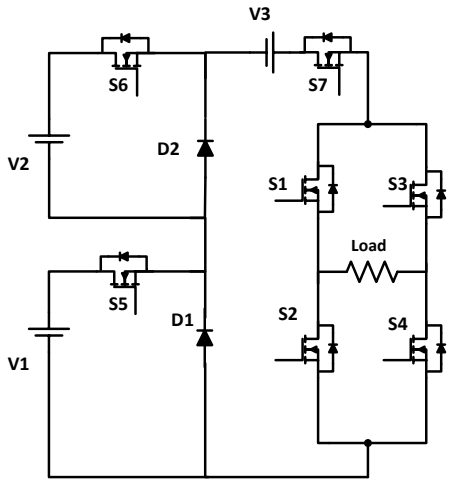

Figure 3. The modified 7-level MLI circuit in [7]

Gajula [29] shows an amazing topology for cascade MLIs as shown in Figure 4. In this topology the maximum output voltage, the number of individual DC sources, the number of switches and the number of diodes is as in above circuit but in this topology only one switch is at on state in each level of output voltage with a reduced number of diodes in each level that are inversely proportional with number of levels that lead to reduce the losses of the switches and increase the efficiency.

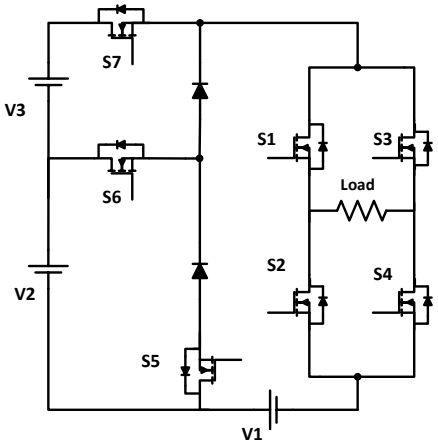

Figure 4. The modified 7-level MLI circuit in [29]

3. THE TOPOLOGY OF THE PROPOSED CIRCUIT

The proposed cascade MLI circuit is shown in Figure 5. In this topology, the maximum output voltage, the number of individual DC sources, the number of switches, and the number of diodes are as in section c. The main difference in this circuit is that only one diode will work at each level, which is the main difference from the circuit in Figure 4. That means fewer losses and higher efficiency.

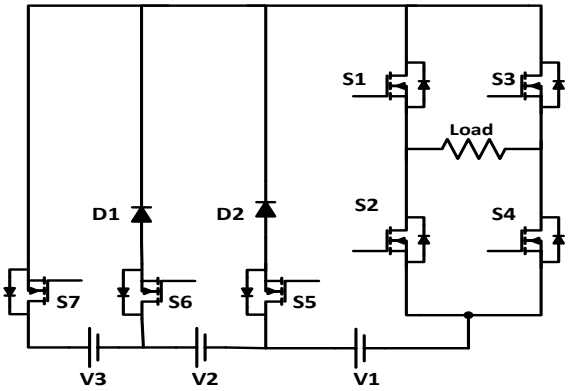

Figure 5. The proposed multilevel inverter circuit

The proposed circuit operates as follows, and only the first 3 modes of operation will be explained as they will be repeated for the rest of the modes:

- At level 1, the load receives energy from the DC source V1 via the switch S5 and the diode D2 on a positive half-cycle basis. For the H-bridge, S1 and S4 are turned on, as seen in Figure 6(a).
- At level 2, Energy is received by the H-bridge via the switch S6 and D1 from the DC sources V1 and V2. Switches S1 and S4 stay on, as seen in Figure 6(b).
- At level 3, through the switch S7, the H-bridge receives energy from the DC sources V1, V2, and V3. Switches S1 and S4 stay on, as seen in Figure 6(c).
- At level 4, the load receives energy from the DC source V1 via the switch S5 and the diode D2 on a negative half-cycle basis. For the H-bridge, S3 and S2 are turned on, as seen in Figure 6(d).
- At level 5, energy is received by the H-bridge via the switch S6 and D1 from the DC sources V1 and V2. Switches S3 and S2 stay on, as seen in Figure 6(e).
- At level 6, through the switch S7, the H-bridge receives energy from the DC sources V1, V2, and V3. Switches S3 and S2 stay on, as seen in Figure 6(f).

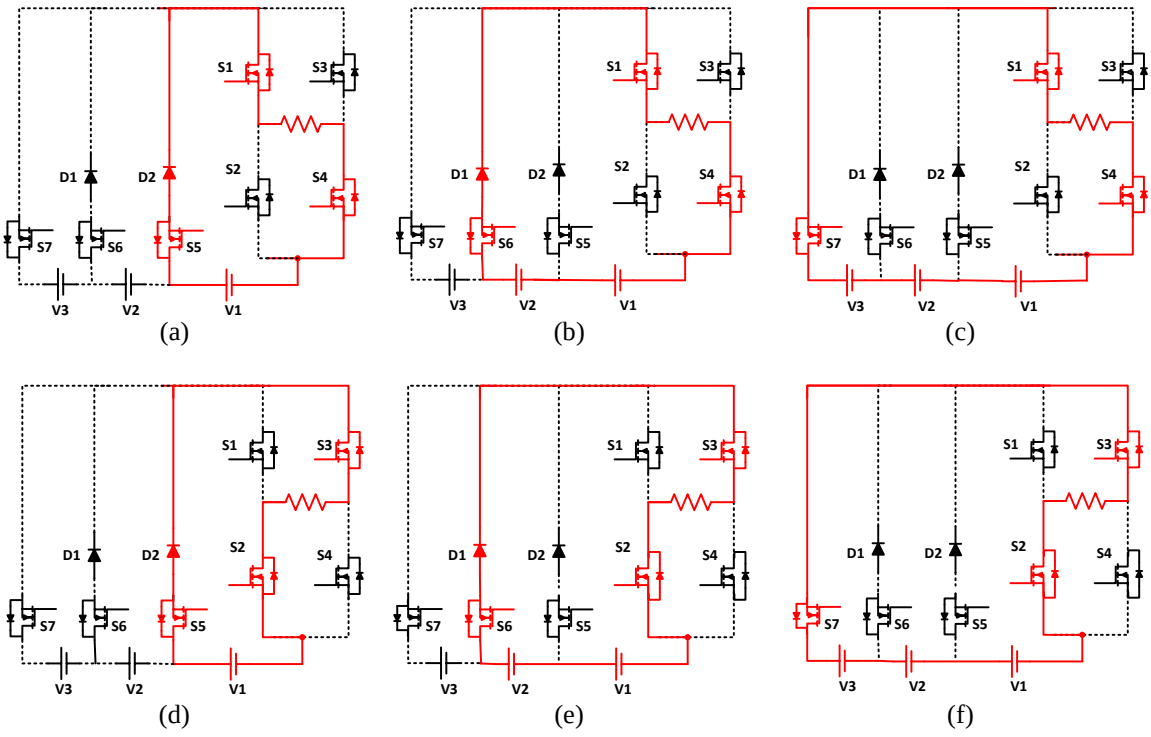

Figure 6. The positive and the negative levels of operation of the proposed inverter (a) level 1, (b) level 2, (c) level 3, (d) level 4, (e) level 5, and (f) level 6

4. SIMULATION MODEL & RESULT OF THE PROPOSED INVERTER

The MATLAB/Simulink model of the proposed inverter is shown in Figure 7. The control circuit generates the gate signals for the switches by comparing a three-phase, 12,250 Hz triangular carrier signal with a 50 Hz sinusoidal reference signal, which is accomplished through the use of the PWM approach. The waveforms of the control circuit are illustrated in Figure 8.

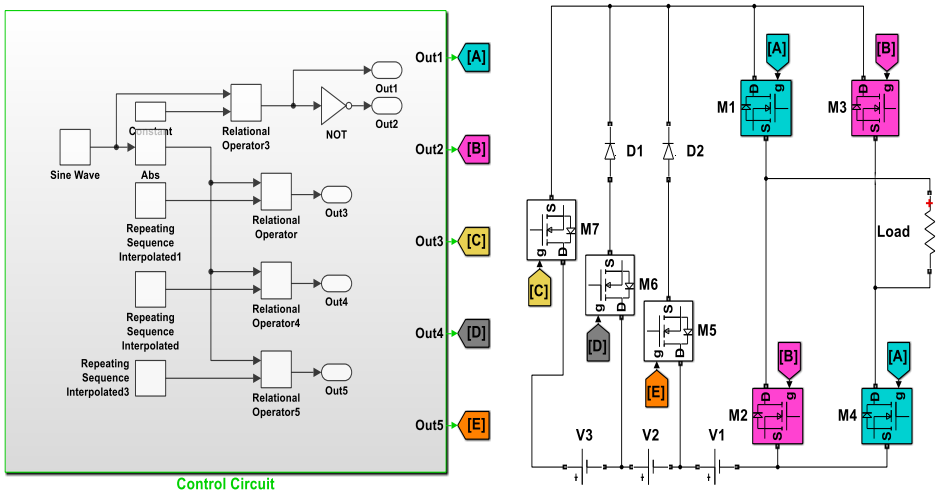

Figure 7. The simulink model of the proposed circuit

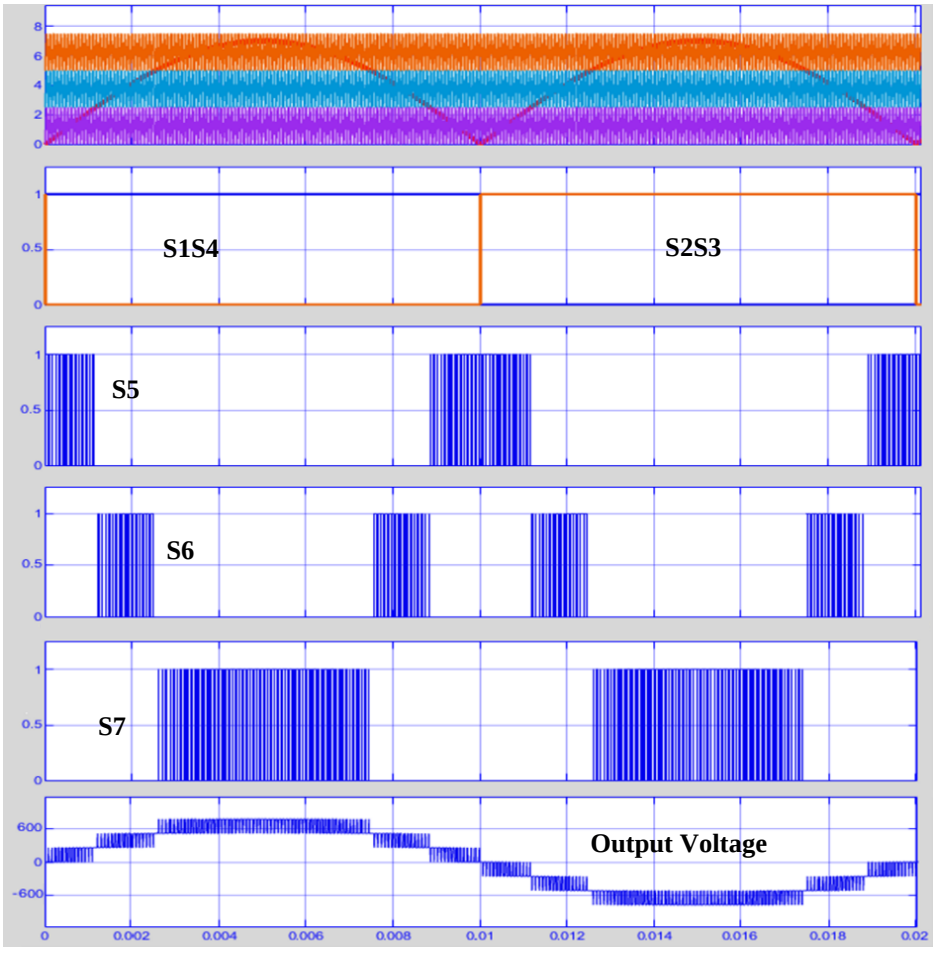

Figure 8. The control circuit waveforms of the proposed topology

Control pulses for the proposed inverter are generated by a series of logical and mathematical MATLAB functions. Output voltage for the proposed 7-levels inverter is shown in Figure 9. The THD for the output voltage is shown in Figure 10, and it can be seen that the THD is about 21.38 when the modulation index m is 0.95.

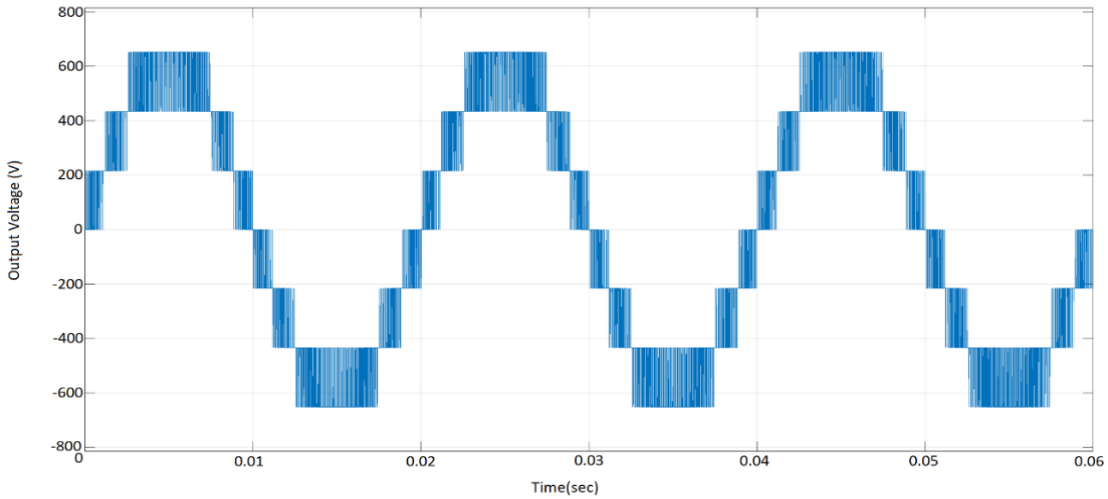

Figure 9. The output voltage of the proposed topology

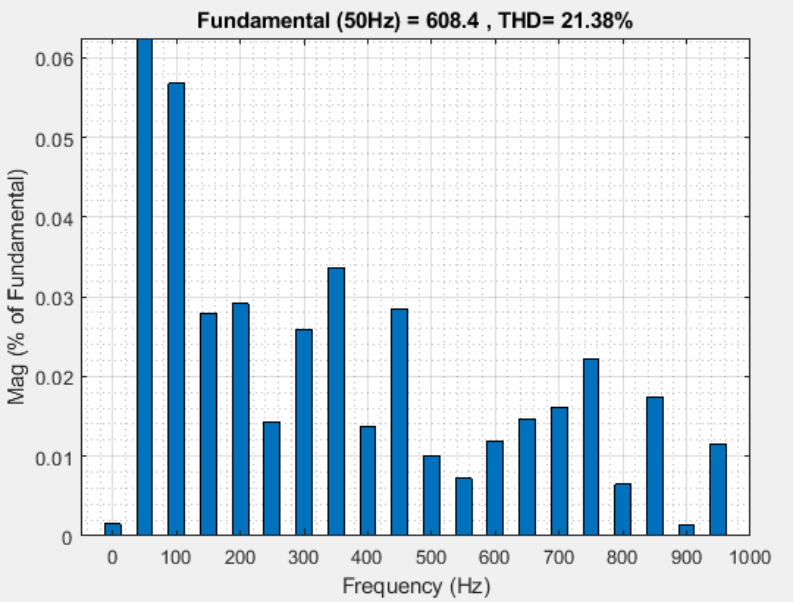

Figure 10. The THD of the proposed topology

For the proposed topology, the number of levels is 7, and for comparison with the inverter circuit that was explained in section c of the previous section, the number of switches is the same. Yet, in the proposed circuit, each level requires one diode and one switch to be in conduction mode. Table 1 shows a comparison between the number of switches in the different topologies for seven-level inverters:

Table 1. The number of switches in the different topologies for seven level inverters

	a-circuit	b-circuit	c-circuit	Proposed circuit
Number of power switches	9	7	7	7
Number of diodes	0	2	2	2

The reduction in switches used leads to a reduction in the size, weight, and cost and an improvement in the efficiency of the converter. The efficiency is also affected by the number of switches in conduction mode in each level of operation. Table 2 shows a comparison between the number of switches during the on-state in the first three levels of operation for the different circuits shown in the previous section.

Table 2. The number of switches in on-mode in the first three levels of operation

	a-circuit		b-circuit		c-circuit		Proposed circuit	
	Power switch	diode	Power switch	diode	Power switch	diode	Power switch	diode
Level 1	5	-	3	2	3	2	3	1
Level 2	5	-	4	1	3	1	3	1
Level 3	5	-	5	0	3	0	3	0

From Table 2, it can be seen that c-circuit and the proposed circuit have the lowest number of switching devices during the on state. On the other hand, the proposed circuit has only one diode working in each operating mode. The reduction of the number of switches (on-state) in the inverter during the operation modes, as well as the reduction of the on-mode, leads to an increase in efficiency. The effect of the switch reduction becomes more significant when adopting a higher number of levels of output voltage. Figure 11 shows the efficiency comparison for the four topologies adopted in this article. This figure shows that the highest efficiency was obtained in the proposed circuit.

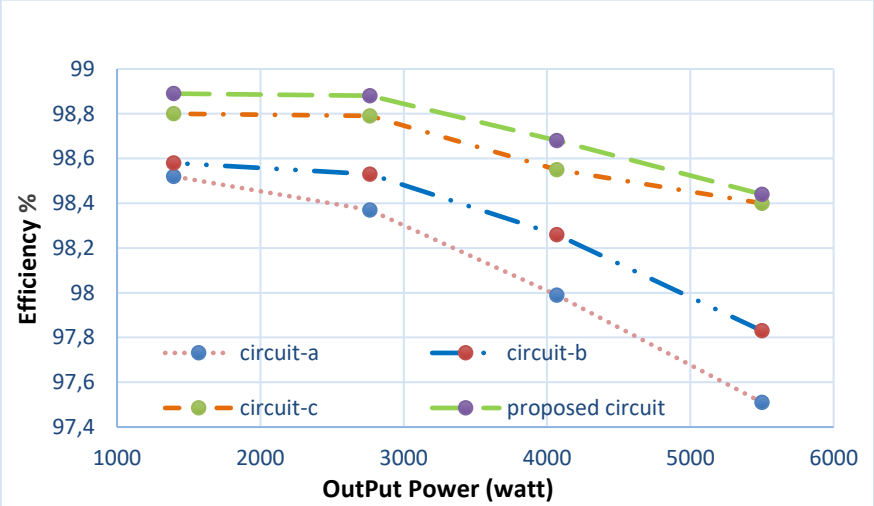

Figure 11. The efficiency comparison

5. CONCLUSION

In today's applications, MLIs are becoming increasingly important. The proposed inverter has the potential to produce a high-quality output voltage while minimizing losses and increasing efficiency. It outperforms the traditional cascaded multilevel inverter in terms of performance. Switching losses are reduced when the suggested control strategy is used, resulting in increased efficiency. According to the simulation results, the new topology is more efficient than the previous inverters.

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