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Performance parameters optimization of CMOS analog signal processing circuits based on smart algorithms

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ABSTRACT

Designing ideal analogue circuits has become difficult due to extremely large-scale integration. The complementary metal oxide semiconductor (CMOS) analog integrated circuits (IC) could use an evolutionary method to figure out the size of each device. The CMOS operational transconductance amplifier (CMOS OTA) and the CMOS current conveyor second generation (CMOS CCII) are designed using advanced nanometer transistor technology (180 nm). Both CMOS OTA and CMOS CCII have high performance, such as a wide frequency, voltage gain, slew rate, and phase margin, to include very wide applications in signal processing, such as active filters and oscillators. The optimization approach is an iterative procedure that uses an optimization algorithm to change design variables until the optimal solution is identified. In this study, different sorts of algorithms the genetic algorithm (GA), particle swarm optimization (PSO), and cuckoo search (CS) are employed to boost and enhance the performance parameters. While decreasing the time required to develop a conventional operation amplifier's settling time. Some studies decrease the value of the power utilized at various frequencies. Others operate at extremely high frequencies, but their power consumption is greater than that of those operating at lower frequencies.

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1. INTRODUCTION

The two main types of integrated circuits (IC) implementation are bipolar and complementary metal oxide semiconductor (CMOS) [1]. In comparison to CMOS technology, bipolar technology is known for having lower noise, better performance at high frequencies, and greater transconductance [2], [3]. Bipolar technology is better than CMOS technology because it has a higher input resistance, uses less power, and can be made on a smaller area of silicon [4]. Using CMOS technology to make an IC is an art form in the field of electronics [5].

Analog IC designers could, for instance, use simulators of circuits such as simulation software with an IC emphasis (SPICE) to evaluate electrical qualities that can be enhanced by adjusting CMOS transistor sizes, and this can be done using an optimization strategy [5], [6]. Increasing CMOS amplifier slew rate, decreasing noise, power, voltage, and layout area, CMOS power gain and other forms of improvement [7], [8]. One of the most important and fundamental things about CMOS is that it can process information very quickly, especially in versions made with modern technology at 180 nanometers, 350 nanometers, and

130 nanometers, as well as its small size, low energy use, and other important characteristics and factors [9]–[11].

In previous years, the bipolar operational transconductance amplifier (OTA) was launched commercially [12]. In both open and closed loop electrical circuits, CMOS OTA has emerged as a crucial component [13]. Operational Transparency According to their input and output, amplifiers are categorized into four groups [14]. The OTA with a single input and a single output, OTA with a differential input, and OTA with a balanced input and differential output [15], [16]. In addition, the current mode technique offers more potential, a wider dynamic range, a simpler circuit design, the lowest power consumption, and a wider signal bandwidth than the voltage mode approach, owing towards its enhanced linearity (bipolar and CMOS technologies) to establish the existing transport circuits [3], [4].

In the sector of analog communications signal processing, current conveyor (CC) circuits are gradually replacing operational amplifiers (op-amps) [17], [18]. Current conveyor second generation (CCII) is a well-known current mode circuit utilized in several applications, including filters and oscillators. In terms of low power consumption, high gain, and other essential characteristics, the work of CMOS amplifiers manufactured using contemporary technologies yields favorable results; nevertheless, this parameter can be enhanced by using methods that have never been utilized in this field before [8], [19]. Using circuit simulators such as SPICE and MATLAB to evaluate the electrical features associated with CMOS technology, metaheuristics have been shown to be beneficial for enhancing analog IC [20]–[22]. The performance parameters of different CMOS OTAs and CMOS CCIIs designs were summarized in this paper. The comparsion of these designs illustrates that low consumption power and wide bandwidth product could be obtained using 0.18 µm CMOS technology and algoritmic process.

2. FUNDAMENTAL OF FOLDED CASCADE CMOS OTA

The Op-amps are advantageous for applications with low frequency, such as video and audio systems [6]. Many analog and mixed-signal circuits, such as Gm-C filters, data converters, regulators, and other high-frequency applications, employ the CMOS OTA as a fundamental building block [23]. Optimising analog IC, especially OTA, remains the most fascinating and demanding task in the world of circuit design [24]. The ideal CMOS OTA is a voltage-controlled current source with constant transconductance and infinite input and output impedances, an example of an OTA is the folded cascade OTA (FCOTA) [10]. Figure 1 illustrates the FCOTA circuit layout (6). It consists of two stages: an NMOS differential pair input stage and a cascade output stage.

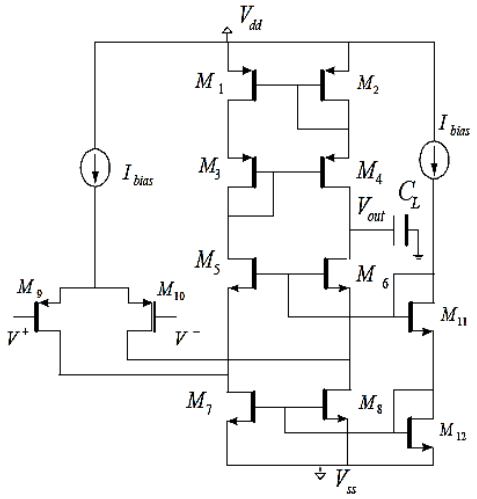

Figure 1. The CMOS OTA folding cascade architecture [25]

An ideal transconductance amplifier is a voltage-controlled current source with infinite input and output impedance that can drive tiny capacitive loads at high frequencies and has an infinite bandwidth [6]. High linearity, high frequency, and low power are the major issues of CMOS OTA [26]. For various purposes, a number of CMOS OTAs with various topologies have been documented [27]. The CMOS FCOTA has a DC gain >80 dB, unity-gain frequency >200 MHz, slew rate >100 V/s, phase margin >50 o,

and a power consumption of 3. The value of the passive components (capacitors and resistors), the length and width of the transistor, and the bias current magnitude and bias voltages are all design factors [19].

– DC in an open loop gain

The open-loop voltage gain of a two-stage op-amp is given by (1):

$$A_V = \frac{g_{M1}}{g_{ds2}+g_{ds4}} . \frac{g_{M6}}{g_{ds7}+g_{ds6}} \quad (1)$$

the transconductance of transistors M1 and M6 are g_{M1} and g_{M6}. The output conductance is g_{ds2}, the transistors transconductance output of (M2, M4, and M7) is g_{ds2} , $g_{ds4,}g_{ds7}$. Respectively.

– Bandwidth-gain

The gives the unity-gain bandwidth (2):

$$GBW = \frac{g_{m1}}{Cc} \quad (2)$$

where Cc is the capacitance of compensation.

– Phase margin

The total of phase shifts provided by the no dominating poles (p1 and p2) and zeros (z) at the unity-gain frequency determines the phase margin of an operational amplifier (3):

$$\text{PM} = \mp 180 - \tan^{-1}\left(\frac{GBW}{\text{p1}}\right) - \tan^{-1}\left(\frac{GBW}{\text{p2}}\right) - \tan^{-1}\left(\frac{GBW}{\text{z}}\right) \quad (3)$$

– Slew rate

The slew rate of this operational amplifier is given by (4):

$$SR = \frac{I_5}{Cc} \quad (4)$$

where I_5 denotes the current flowing through the transistor M5.

– Power consumption

The power consumption of a two-stage operational amplifier has the form (5):

$$P = (V_{DD} - V_{SS})(I_5 + 2I_7) \quad (5)$$

where V_{SS} and V_{DD} are the operational amplifiers power supply and I_7 is the current that flows through transistor M7.

– Area

The sum of the transistor and capacitor areas determines the operational amplifier's area A (6):

$$Area = \sum_{i=1}^{k} W_i . L_i \, 0 \quad (6)$$

where W_i and L_i are lengths and widths of MOSFET gate transistors [19].

3. FUNDAMENTAL OF CMOS CCII

Figure 2 depicts a current conveyor with three active ports: X, Y, and Z. Its primary purpose is to generate a current follower between ports Z and X using the translinear loop formed by transistors M1-M4 [28]. Current mirrors M5-M6 and M7-M8 can be used to create a voltage follower between ports Y and X. The current conveyor topology is the most preferred due to its higher performance and the need to implement a translinear loop [29]. As a consequence, the optimization of the CCII's design takes into account its primary functions: parasitic resistance at port X(R_X) and cutoff frequency (f-3dB) [30]. Remember that the purpose is to get low input resistance by lowering the first objective and large bandwidth by optimizing the second [31]. L and W is the length of channel and width of gate respectively are the geometrical dimensions that define all transistors. The design challenge can be stated as follows: $R_X(X)$ and $f_{-3dB}(X)$ (7).

$$X = \{W_n, W_p, L_n, L_p, I_0\} \tag{7}$$

subject to (8):

$$g_{1,2}(X) \leq 0 \tag{8}$$

the resistance R_X is (9):

$$R_X = \frac{1}{g_{mn} + g_{mp}} = \frac{1}{\sqrt{2\mu_n C_{ox}\frac{W_n}{L_n} I_0} + \sqrt{2\mu_p C_{ox}\frac{W_p}{L_p} I_0}} \tag{9}$$

where $g_{mn}\ and\ g_{mp}$ the NMOS and PMOS transistors transconductances respectively, C_{ox} is the gate oxide capacitance. The bias current is I_0. μ_n the electrons mobility and μ_p the holes mobility.

The cut–off frequency is (10):

$$f_{-3dB}(X) = \frac{\omega_{-3dB}}{2\pi} \tag{10}$$

The saturation constraints are g_1 and g_2 are shown in by:

– The constraint of M2 and M8 transistors (11):

$$g_1 = V_{SS} - V_X(min) + V_{tn} + \sqrt{\frac{2I_0}{\mu_n C_{ox}\frac{W_n}{L_n}}} + \sqrt{\frac{2I_0}{\mu_p C_{ox}\frac{W_p}{L_p}}} \tag{11}$$

– The constraint of M4 and M5 transistors (12):

$$g_2 = V_X(max) - V_{DD} - V_{tp} + \sqrt{\frac{2I_0}{\mu_n C_{ox}\frac{W_n}{L_n}}} + \sqrt{\frac{2I_0}{\mu_p C_{ox}\frac{W_p}{L_p}}} \tag{12}$$

The threshold voltage of (NMOS) , (PMOS), and supply voltages are (V_{tn}) (V_{tp}), (V_{DD}), (V_{SS}) respectively and $W_n\ (W_p), L_n(L_p)$. Are the gate width and the length of channel for (p channel) (n-channel) transistor, respectively. The $V_X(min)$, $V_X(max)$ is the minimum and maximum value of voltage. These is mathmetical for CMOS current conveyor second generator CCII. After this the famus algorithm that it used with such teqnique is discussed.

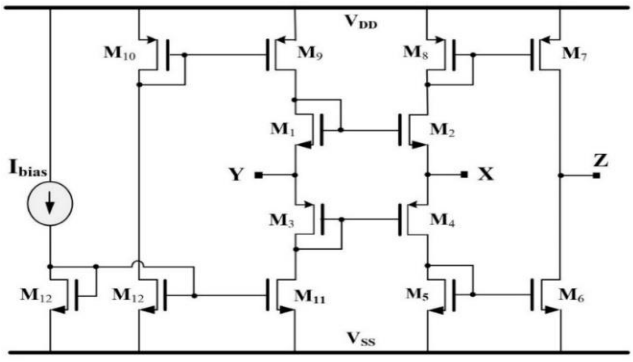

Figure 2. CMOS current conveyor second generator CCII [32]

4. SMART ALGORITHMS

One important way to improve many performance parameters, like unit product gain, reducing power consumption, and slew rate, is to use smart algorithms [5], [33]. Based on these algorithms can be performance parameters optimization of CMOS analog signal processing circuits. The main ones are the particle swarm optimization (PSO) and cuckoo search (CS) algorithms. Which have high performance of some parameter.

5. PARTICLE SWARM OPTIMIZATION ALGORITHM

The social behavior of fish and birds is described by a mathematical model based on the basic properties used to describe complex systems of self-regulation [12], [34]. This model was developed by Kennedy and Eberhart in 1995 and called PSO. Currently, the PSO is used to solve optimization problems significantly and successfully because of a single goal algorithm [15]. The PSO algorithm is represented by a finite search space that contains a set of randomly distributed particles that have a certain velocity and position that are represented by simple mathematical models. These models represent every movement of the particles to be the best place in the search space or the best place as an individual, in addition, there are different rules for updating different variables [35]. The main idea is to provide a search space containing an array of particles, and in addition to setting the initial velocity vector, it gives them a suitable initial position [36]. Depending on certain parameters randomly in order to set the velocity, and during this process, the particle position is changed in each iteration [27]. Each particle has the ability to determine best position and whether its current location is superior to the positions of other particles. According to the math in (13) and (14), the positions and speeds of the particles must be changed based on what is shown in Figure 3.

$$\mathrm{vi}(t+1) = \mathrm{vi}(t) + \mathrm{c1rand}()(\mathrm{pbest}(t) - \mathrm{pi}(t)) + \mathrm{c2rand}()(\mathrm{gbest}(t) - \mathrm{pi}(t)) \quad (13)$$

$$\mathrm{pi}(t+1) = \mathrm{pi}(t) + \mathrm{vi}(t+1) \quad (14)$$

where pi (t+1) and vi (t+1) represent the particle position and velocity in the ith iteration, respectively. A function that returns the value of a real random regular number between 0 and 1 is rand (). gbest and pbest represent the best global position among all the particles and the particles' best position; c1 and c2 are parameters representing the particle dependence (perception) and social behavior in the swarm, respectively. These constants are the most closely related in (13), and as shown a number of tests have shown that the convergence is faster the higher the value of the constants [37]. The values of c1 and c2 are important in improving performance depending on the type of problem. The best performance of the PSO algorithm is if the value of the constants c1=c2=2 is set as shown in Figure 3 [6], [15].

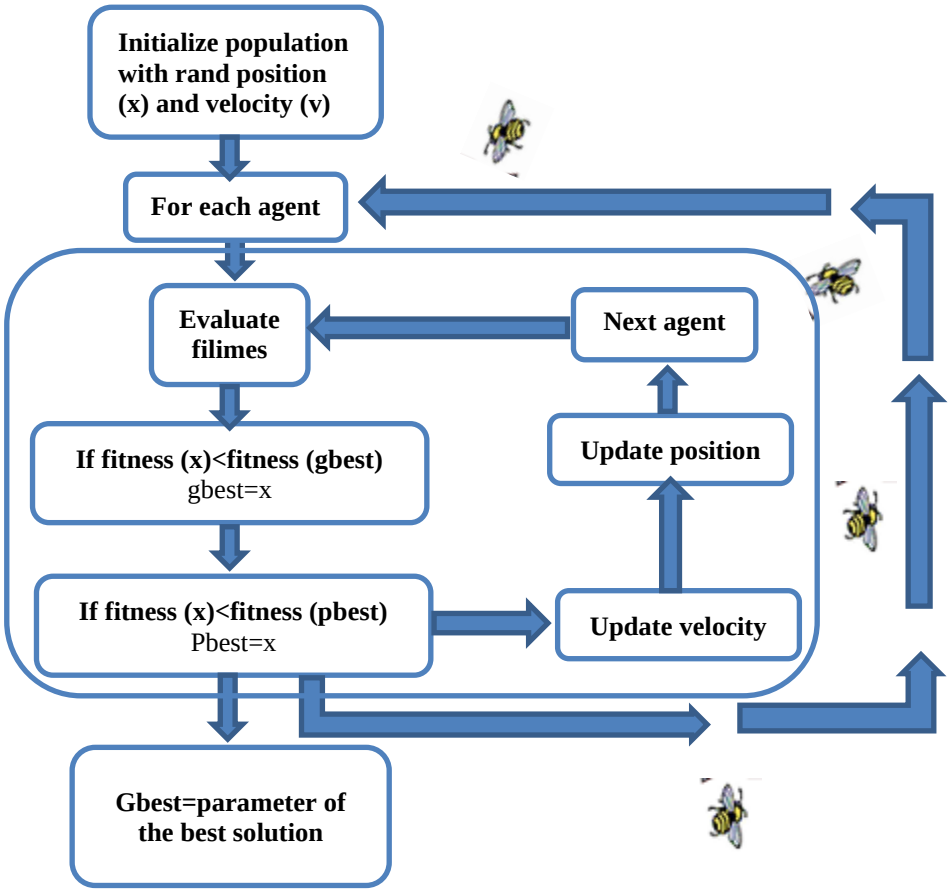

Figure 3. The PSO algorithm flowchart [34]

6. CUCKOO SEARCH ALGORITHM

The CS algorithm is comparable to other algorithms, such as differential evolution (DE), PSO, and genetic algorithm (GA) which are classified as being random [4], [6], [38]. It is one of the algorithms that rely heavily on population. In this algorithm, each individual element is connected to the cuckoo egg, and each pattern is associated with the nest [39]. This algorithm uses a special approach that is similar to the HS algorithm, in which the mechanism of selection or elitism is utilized [40]. Based on several typical measurement functions, the CS algorithm was proposed, and its performance was compared to that of the PSO and DE algorithms in [11], [37]. In randomization, the performance of the CS algorithm was shown to be superior to that of the DE and PSO algorithms [34], [41]. In addition, the researchers observed that the number of parameters that the CS algorithm must adjust is far lower than the number of parameters required by other types of algorithms [42]. The common operation of the CS algorithm is represented by the following (15):

$$\mathrm{Xg}+1,\mathrm{i}=\mathrm{Xg},\mathrm{i}+\alpha\otimes Lévy(\lambda) \quad (15)$$

Here, the i^{th} cuckoo of the current solution is X_g of iteration g, $X_{g+1,i}$ is the i^{th} cuckoo of the new solution, and g is the current generation number [36], [39]. α is the size of step which depends on interests problem scales. Lévy(λ) is a random path generated by Lévy flight, and Lévy is obtained from a Lévy distribution with an infinite mean and an infinite variance, as shown in (16) [43]. The random walk algorithm is more efficient than the PSO algorithm. "Product" refers to the multiplication performed inside [10], [44].

$$Lévy\sim u\ =\ t-\lambda \quad (16)$$

where u is normal distribution and t is CS generation, λ is considered in the range (1, 3). The Mantegna algorithm is used to produce the Lévy path. Following a random walk is the size of the steps [45]. With a force law distribution featuring heavy tails [27].

7. LITRECHURE REVIEW

The following Tables 1-3 illustrates the OTA's performance for the years (2012-2021) with and without using various algorithms, and for overall references from 2012–2022 of CCII. These tables content important parameters with are used in high frequency application, as DC gain (dB), bandwidth of unity gain (MHz), phase margin (degree), type of algorithm, slew rate(mV/μs), chip area μm^2, consumption power mw, and technology (channel length) (μm). In Table 1, there are numerous publications, each of which focuses on or is interested in a specific aspect, such as power consumption, slew rate, and gain bandwidth product. To reduce power consumption, the authors in [9] employs the CS algorithm, where power consumption is as low as possible compared to other research. As for bandwidth, the search results using the PSO algorithm are excellent, and packets have been significantly enhanced in [2]. The majority of research uses high frequencies at the expense of energy.

Table 2 displays the research group that does not employ a specific algorithm. The lowest value of energy consumed was 144.3 nanowatts in 2010 study, and the maximum bandwidth they were able to achieve was 485 MHz in 2013. Several researches are listed in Table 3, some of which depend on a certain type of algorithms and others on the sort of technology used to nationalize the system. In comparison to other studies, research conducted in 2013 is regarded as the most effective in terms of reducing energy consumption.

Table 1. Presented a summary of the performance parameters of several types of CMOS OTA designs based on algorithmic processes for the years 2012-2020

Refrences	DC gain (dB)	Bandwidth of unity gain (MHz)	Phase margin (degree)	Type of algorithm	Slew rate (mV/μs)	Chip Area μm^2	Consump-tion power mw	Technology (channel len-gth) (μm)
Samir Barra *et al.* [1]	96	2,5	70°	MOGA	2,25	89	0.047	0.18
B.Mohammad *et al.* [2]	84.33	543.3	51.34°	PSO	534	-----	1.2	0.18
Benhala and Ahaitouf [9]	85.58	-----	-----	GA	3.676	-----	5.23	0.5
Dendouga *et al.* [12]	76	1.5	70°	MOGA	2250	559	0.047	0.18
Prajapati and Shah [13]	59.19	20.03	63.53°	PSO	18350	28.52	0.184	0.18
Prajapati and Shah [13]	50.49	16.38	50.09°	PSO	20130	97.81	0.349	0.35
Prajapati and Shah [14]	91.39	0.14555	68.87°	PSO	11900	4839.8	0.01492	0.18
Motlak and Mohammed [15]	82	6.27	89.6°	PSO	3155	-----	0.485	-----
Salhi *et al.* [16]	88.95	83.653	55.202	IWO	27.5	-----	0.5796	-----
Prajapati and Shah [17]	76.17	0.02021	45.43°	CS	22060	5409.4	0.000278	0.18
Prajapati and Shah [17]	85.04	0.06004	73.69°	CS	12430	3458	0.000863	0.35

Table 2. Different OTA designs were summarized without the use of an algorithm

Refrences	DC gain (dB)	Bandwidth of unity gain (MHz)	Phase margin (degree)	Slew rate (mV/μs)	Chip area (mm^2)	consumption power (mW)	Technology (channel length) (μm)
Mukahar and Jubadi [20]	48.8	9.32	-----	-----	0.089	4.88	0.5
Pereira-Arroyo *et al.* [44]	-----	-----	-----	3.676	-----	0. 1443	-----
Laajimi *et al.* [45]	57	55	62°	0.1	-----	2.27	-----
Bakawale *et al.* [30]	-----	-----	55°	-----	0.025	14.2	-------
Lee *et al.* [46]	87	485	70°	------	-----	8	0.35
Yodtean [37]	76	423	86°	-----	0.4	0.00458	0.18
Mirković *et al.* [47]	57.6	140	83°	190000	-----	9.77	0.350
Daoud *et al.* [26]	46	14	85°	-----	-----	0.028	0.18
Abdelfattah *et al.* [48]	46	3.6	56°	-----	-----	-----	0.35
Akbari and Hashemipour [38]	96	11	76°	96	-----	0.4	0.18
Garradhi *et al.* [43]	42.58	247.3	92°	------	-----	0.5	0.090
Yang and Roberts [49]	52	4,8	57°	5	-----	3.72	130
Patel and Thakker [27]	44.5	18.7	60.5°	-----	-----	-----	-----
Sabry *et al.* [50]	32	3.95	70°	-----	-----	-----	0.18
Dong *et al.* [51]	-----	9.76	71.7°	2.76	0.213	29.46	-----

Table 3. Illustrate the overall references from 2012–2022 of CCII

Refrences	Type of algorithms	Technology (channel length) (μm)	Supply voltage (V)	Bias current (μA)	Maximum frequency (MHz)	Consumption power (mW)
Bakawale *et al.* [30]	----	----	1.12	-----	25	14.2
Broomandnia *et al.* [31]	-----	0.18	±0.6	-----	0.006	0.191
Gajjar and Patel [32]	-----	0.18	1.8	4	-----	0.070
M'Harzi *et al.* [52]	-----	0.35	±1.5	100	-----	1.28
Garbaya *et al.* [53]	RBF-PSO	-----	-----	-----	-----	-----
Yakout and Alawadi [54]	-----	0.8	±2.5	300	-----	4.86
Lberni *et al.* [55]	NSGA II and MOGA	0.18	±1.8	80	6600	-----
Mallick *et al.* [56]	CRPSO	0.18	±2.5	-----	-----	-----

8. CONCLUSION

Numerous applications utilize high frequencies, and compared to low frequencies, their power consumption is greater; however, some studies underestimate the power consumed at various frequencies. High bandwidth, phase margin, spin rate, and voltage gain, which are performance parameters for CMOS OTA and CMOS CCII. This parameter was enhanced by the use of cutting-edge (180 nm) nanoscale transistor technology. Second, different types of algorithms such as CS, PSO, and GA are utilized. Using PSO, the maximum bandwidth available is equal to 543.3 MHz. The minimum power consumption in CMOS OTA is 278 uW, whereas in CMOS CCII it is 70 uW.

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