

An maximum power point tracking interface circuit for low-voltage DC-type energy harvesting sources

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ABSTRACT

This paper presents a maximum power point tracking (MPPT) interface circuit for low-voltage DC-type energy harvesting sources such as light and thermal energy. Most energy harvesting systems used in miniature-sized sensor systems require start-up circuits because the output voltages of small-sized energy transducers are very low and not enough to directly power electronic systems. The proposed interface circuit is driven directly by the low output voltages of small size energy transducers, eliminating the need for complex start-up circuitry. A simple MPPT controller with the fractional open-circuit voltage (FOCV) method is designed and fabricated in a 65-nm complementary metal oxide semiconductor (CMOS) process. Measurement results show that the designed circuit can track the MPP voltage even in the presence of the open-circuit voltage fluctuations and can operate properly at operating voltages as low as 0.3 V. The interface circuit achieves a peak power efficiency of 97.1% and an MPPT accuracy of over 98.3%.

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1. INTRODUCTION

Harvesting environmental energy for self-powering has become a necessity in ultra-low power and compact sensing systems such as wireless sensor nodes and implantable devices [1], [2]. Light [3]-[5], vibration [6], [7], thermal [8], [9], and radio frequency (RF) energy [10] are being utilized as the main energy sources for energy harvesting. The environmental energies are usually transduced into electrical energy using energy transducers such as photovoltaic (PV) cells, piezoelectric transducers (PZTs), thermoelectric generators (TEGs), and rectifying antennas. These transducers, except PZTs, generate DC-type output signals.

An energy transducer has a maximum power point (MPP) that outputs the maximum available power. Maximum power point tracking (MPPT) is required because the MPP changes in real time due to changes in the surrounding environment [11]-[14]. The MPPT is even more important in miniature-sized systems because size-limited energy transducers can only produce extremely small output power due to limited power density down to a few $\mu\text{W}/\text{cm}^2$. Therefore, it is crucial to extract as much power as possible from the energy harvester while the additional power dissipated by the MPPT circuit should be minimized [15]. Among various techniques for MPPT, the fractional open-circuit voltage (FOCV) method [16] has been commonly used for micro-energy harvesting systems because it is simple and thus has advantages in terms of additional power consumption and implementation complexity. Since the MPP voltage of an energy converter is a fraction of the open-circuit voltage, the MPP voltage can be obtained by periodically sampling the open circuit voltage.

One specific issue of small-sized energy transducers is that they usually generate very low output voltages. Single PV cells [17] have output voltages less than 500 mV, and commonly used TEG devices [8] can generate output voltages in the range of 10 mV/K to 50 mV/K. As a result, they may not be enough to drive the MPPT interface directly and some kind of startup circuitry is required. Several start-up techniques have been reported: utilizing a mechanical switch [8], a pre-charged battery [18], an off-chip transformer [19], a Colpitts oscillator [20], and post-fabrication processes [21]. However, these techniques are not suitable for self-powered small size sensing systems as mentioned in [9].

In this study, we try to drive the MPPT interface circuit for DC-type energy harvesting sources by using the low output voltages of the transducers without complex start-up circuitry. With the recent advances in integrated circuit processing technology, the driving voltage supplied to electronic systems is on the decline. In keeping with this, various techniques for operating circuits at low voltages have been developed [22]. The continuous development of these process technologies and low-voltage circuit techniques is expected to make it possible to implement an energy harvesting system that can be driven directly with low output voltages from energy transducers.

In this design, a 65 nm complementary metal oxide semiconductor (CMOS) process has been used, and energy transducers that output an open-circuit voltage of 0.6~1.2 V have been targeted. Therefore, the proposed circuit has been designed to operate even at a voltage as low as 0.3 V. Since the proposed circuit should operate at 0.3 V that is lower than the threshold voltage of a regular transistor provided in the process used in this design, various low-voltage circuit techniques must be applied. The low-voltage circuit design techniques applied in this design are as follows: operation in weak inversion, using a bulk-driven differential pair, using composite transistors, and using distributed transistor arrays. The proposed circuit can be applicable to energy transducers with lower output voltages if a finer and advanced process is used. In section 2 the overall architecture of the proposed system and the design of its component blocks are presented. Experimental results and conclusions are presented in sections 3 and 4, respectively.

2. PROPOSED MPPT INTERFACE CIRCUIT

2.1. Overall architecture

The block diagram of the proposed MPPT interface circuit for low-voltage DC-type energy sources is shown in Figure 1. It consists of an energy transducer (a PV cell or a TEG), two PMOS switches (SW1, SW2), a storage capacitor (C_{STO}), and an MPPT control block. The MPPT control block generates a periodic signal MC, and while MC is '1', the switch SW1 is opened so that the open-circuit voltage (V_{OC}) of the energy transducer is sampled and stored. While MC is '0', the energy harvested energy is stored in C_{STO} . At this time, the voltage V_{STO} becomes equal to the output voltage of the energy transducer (V_{PV} or V_{TEG}) and should maintain a value near the MPP voltage (V_{MPP}) in order to harvest the maximum available power. For this, the MPPT controller generates a signal EN to control the power switch SW2. While EN is '0', SW2 is turned on, and the harvested energy is transferred to the load.

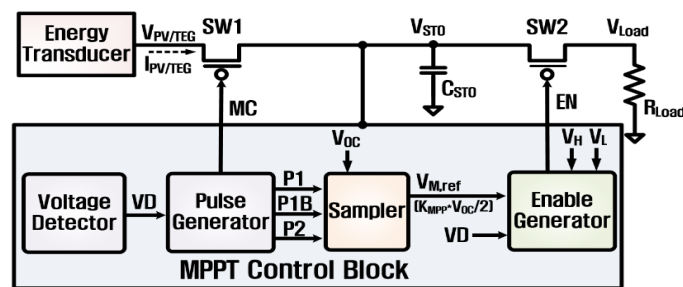


Figure 1. Simplified block diagram of the proposed MPPT interface circuit

The power obtained from miniature-sized transducers is usually not enough to operate the load (e.g. sensor nodes). Therefore, efficient power management is required to resolve the power inconsistency. In this design, the active/sleep technique [6], [9] is employed to solve the problem. The load (R_{Load}) switches between active and sleep mode, and the operating duty cycle varies depending on the amount of energy the circuit can harvest. MPPT is performed by adaptively connecting C_{STO} to the load through on/off operation of SW2. When SW2 is on, the energy stored in C_{STO} is supplied to the load, and the application load wakes up and starts working. The target application load is a system that can be driven directly with the voltage V_{Load} .

obtained from an energy transducer with a low output voltage. However, in the case of a load system that is difficult to drive directly with V_{Load} , it can be driven with a boosted voltage through a boost converter. In this case, the load of the proposed circuit can be a DC-DC boost converter.

2.2. Pulse generator

For MPPT control, MPPT pulses (MC, P1, P1B, P2) are generated by the pulse generator shown in Figure 2(a). The clock generator generates a clock signal (CLK) with a frequency of about 50 Hz. The MC pulse is generated once every 128 cycles of CLK as shown in Figure 2(b). The pulse signals P1, P1B, and P2 required for sample/hold operation of the sampler are also generated based on the MC signal. When MC is '1', that is, while sampling the open-circuit voltage of the energy transducer, the voltage level of the MPPT pulses is converted from V_{STO} to V_{OC} to properly turn the switches on and off. The detailed timing diagram of these control signals is shown in Figure 2(b).

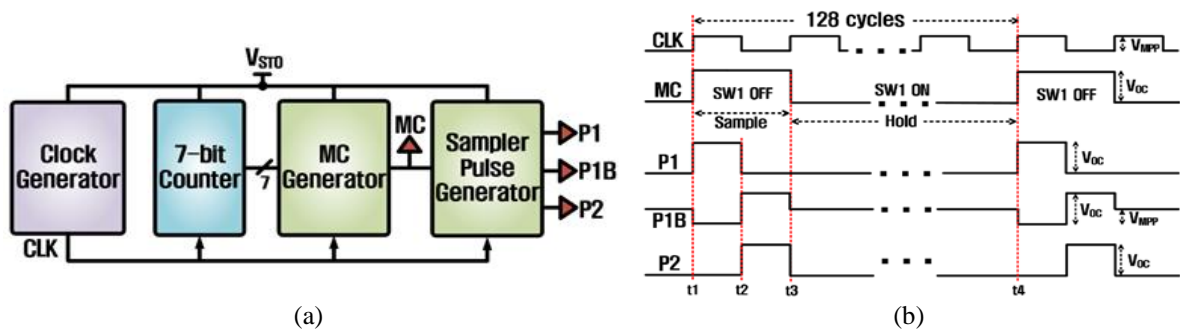


Figure 2. Pulse generator (a) architecture and (b) timing diagram of MPPT pulses

2.3. Sampler

The sampler samples the open-circuit voltage of the energy transducer and then generates an MPPT reference voltage ($V_{M,ref}$) and feeds it to the enable generator. In practice, a reference voltage which corresponds to $V_{MPP}/2$ instead of V_{MPP} is used for the proper operation of internal circuits. For low-voltage operation, the sampler is implemented with only switches and capacitors as shown in Figure 3. Compared to the conventional sampler [9] implemented by using an operational amplifier, the sampler designed in this paper is better for low-power and low-voltage characteristics.

The designed sampler consists of a PMOS switch (SW_{SH1}), two NMOS switches (SW_{SH2} , SW_{SH3}), and two capacitors (nC_{SH} , mC_{SH}). During the P1 phase as shown in Figure 2(b), the V_{OC} of the energy transducer is sampled on the sampling capacitor nC_{SH} by closing SW_{SH1} . At the same time, the holding capacitor mC_{SH} is discharged by closing SW_{SH3} to refresh the reference voltage $V_{M,ref}$. Then, during the P2 phase, the charge of nC_{SH} is shared with mC_{SH} by closing SW_{SH2} , setting $V_{M,ref}$ to the following desired value:

$$V_{M,ref} = \frac{1}{2}V_{MPP} = \frac{1}{2}K_{MPP}V_{OC} = \frac{n}{n+m}V_{OC} \quad (1)$$

here, the K_{MPP} for PV cells usually ranges from 0.6 to 0.8 [23], in our case 0.7. The K_{MPP} for TEGs is 0.5 [8].

In this prototype design, external capacitors are used to facilitate the generation of a more stable reference voltage and the generation of different values depending on the energy source. The C_{SH} value is set to 1 nF. In order to generate a reference voltage of $V_{MPP}/2$, in the case of light energy, the n value of the sampling capacitor is set to 7, and the m value of the holding capacitor is set to 13. For thermal energy, n is set to 1, and m is set to 3. The switches SW_{SH1} and SW_{SH2} are implemented using regular- V_t MOS transistors, while the switch SW_{SH3} is implemented using a high- V_t MOS transistor having a higher threshold voltage to minimize the variation of the $V_{M,ref}$ due to the leakage current in the holding mode. The switch transistors have been carefully sized for the accuracy and speed of the sampling, charge sharing, and holding operation.

2.4. Voltage detector

The voltage detector shown in Figure 4 is used to deactivate the MPPT control block until the voltage V_{STO} charged in C_{STO} reaches a threshold value. This is to prevent unnecessary current consumption and minimize the leakage of charges stored in C_{STO} . The threshold value can be adjusted using a resistor divider consisting of R_{S1} and R_{S2} , which is set to 250 mV in this design. The detector compares the voltage

$V_{STO,div}$ generated by the resistor divider with the reference voltage V_{REF} of about 100 mV and outputs VD, the enable signal of the MPPT control block. In order to reduce the sensitivity to noise, it is designed to have a hysteresis function using positive feedback composed of R_{E1} and R_{E2} .

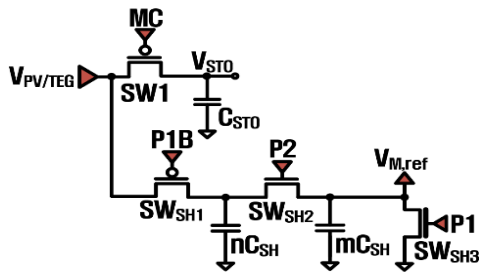


Figure 3. Sampler

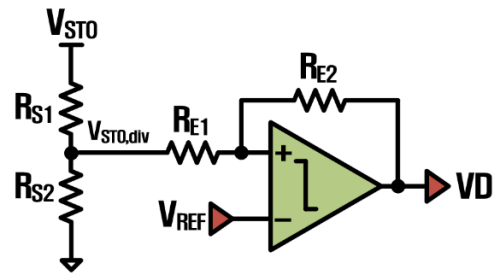


Figure 4. Voltage detector

2.5. Enable generator

The enable generator consists of a resistor string, two comparators, and a latch as depicted in Figures 5(a) and (b). The resistor string generates a predetermined maximum MPP level (V_H), and a predetermined minimum MPP level (V_L), and supplies them to the comparators. V_H and V_L are set to $V_{MPP}/2 + \Delta V$ and $V_{MPP}/2 - \Delta V$. ΔV is a small value and its specific value is not critical for the band-band control. In this design, $2\Delta V$ is set to a value corresponding to about 5% of V_{STO} . The output signals of the comparators are fed into the latch to create a signal EN that determines the on or off state of SW2, defining the charging and discharging phases.

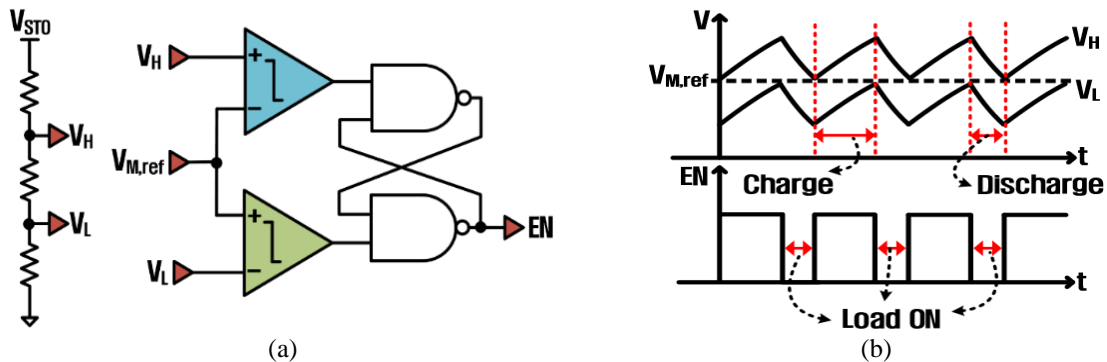


Figure 5. Enable generator (a) architecture and (b) detailed waveforms of the band-band control

When C_{STO} is charged and V_L reaches $V_{M,ref}$, EN goes low and SW2 is turned on. During this discharging phase, the energy stored in C_{STO} is supplied to the load, and the application load begins to operate. When C_{STO} is discharged and V_H reaches $V_{M,ref}$, EN goes high and SW2 is turned off. During this charging phase, the transfer of energy to the load stops, and one operation cycle is completed. When C_{STO} is recharged again, the cycle of operation repeats. Thus, C_{STO} is repeatedly charged and discharged near the V_{MPP} , and the energy transducer always operates near the MPP.

2.6. Comparator and reference circuit

The comparator used in the enable generator and voltage detector is shown in Figure 6. The basic structure of the designed comparator is based on the CMOS Miller OTA proposed in [24]. Since the comparator should operate at a voltage as low as 0.3 V, several low-voltage circuit design techniques have been employed. First, a bulk-driven differential pair operating in weak inversion consisting of M1, M2, and M8 is used as the input stage. The bulk-driven differential pair is advantageous for low-voltage operation because it can obtain a larger signal swing compared to the gate-driven one [25].

Second, in weak inversion an important configuration for a MOS transistor is a composite transistor [26]. The composite transistor operating in weak inversion has the effect of improving the output resistance

to the extent that can be achieved with a cascode transistor structure. The transistor pair M3-M5 and M4-M6 form composite transistors and act as the active load of the differential pair. In addition, transistors M3 and M4 perform a dc-level shifting function so that the input transistor M11 of the second amplification stage can operate properly without an additional DC bias voltage.

Finally, the distributed transistor array technique [27] is used to implement all transistors of the comparator. In sub-micron CMOS processes, halo implants are usually used to reduce the short channel effect. However, this leads to a decrease in the output resistance of the transistors and an increase in the threshold voltage mismatch [28]. A simple approach to alleviate the reduction in output resistance is to use an array (series-parallel association) of unity transistors instead of single large device. The output resistance of a $s \times p$ array of unity transistors can be s times greater than that of a unity transistor while the transistor array is equivalent to a single halo-implanted transistor in its threshold voltage characteristics [29]. The unity transistor aspect ratio and $s \times p$ array information for each transistor used in this comparator design are shown in Table 1. The designed comparator shows a dc gain of 40 dB, a 3 dB frequency of 160 Hz, and a current consumption of 27 nA at a supply voltage of 0.25 V.

A reference circuit is required to supply stable currents to the clock generator and comparators, and to supply a reference voltage to the voltage detector. The reference circuit designed based on the beta multiplier reference [30] is shown in Figure 7. The basic beta multiplier circuit consisting of M1~M4 and R1 has very poor sensitivity to the supply voltage changes due to the low output resistance of the short channel transistors. To increase the output resistance a feedback configuration using a simple amplifier consisting of M5~M8 is adopted. In addition, the distributed transistor array technique used in the comparator design is also employed in the reference circuit design to increase the output resistance of short-channel transistors and thus improve the circuit performance at low voltages. The reference circuit includes a start-up circuit consisting of M9, M10, and C1 which consumes no power after start-up [31]. Simulation results have shown that the designed reference circuit operates at a supply voltage of 0.2 V or more, and outputs a reference current of 5 nA and a reference voltage of 100 mV. The reference current and voltage sensitivity to the power supply are 0.3 nA/V and 6 mV/V, respectively, and the current consumption is 17 nA.

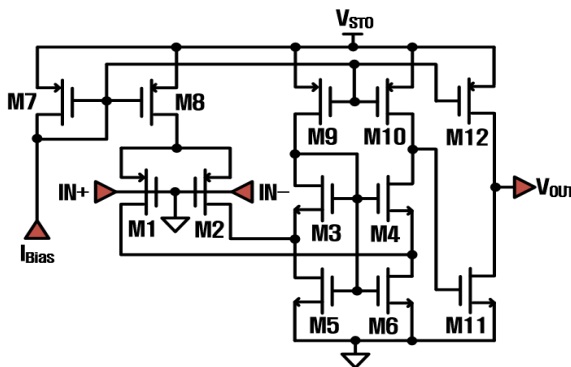


Figure 6. Low-voltage comparator

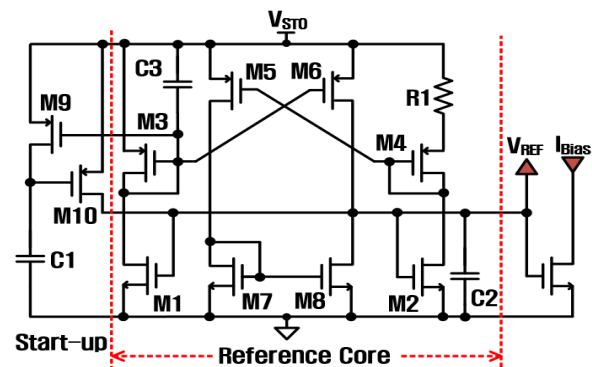


Figure 7. Low-voltage reference circuit based on beta multiplier

Table 1. Transistor aspect ratio of the comparator

Transistor	$s \times p \times (W/L) (\mu\text{m}/\mu\text{m})$	Transistor	$s \times p \times (W/L) (\mu\text{m}/\mu\text{m})$
M1, M2	$10 \times 12 \times (5/1)$	M3, M4	$15 \times 30 \times (2/1)$
M5, M6	$15 \times 8 \times (2/1)$	M7	$15 \times 20 \times (5/1)$
M8	$15 \times 60 \times (5/1)$	M9, M10	$15 \times 8 \times (5/1)$
M11	$21 \times 8 \times (2/3)$	M12	$15 \times 20 \times (5/1)$

3. RESULTS AND DISCUSSION

The proposed circuit has been fabricated using a 65-nm CMOS process. The layout and photograph of the designed chip is shown in Figure 8. Its active area is $720 \mu\text{m} \times 640 \mu\text{m}$. The performance of the fabricated chip has been verified for light energy and thermal energy.

3.1. Measurement results for light energy

Figure 9 shows the experimental setup for photovoltaic energy harvesting. The PV cell used for the

measurement is SOLARBOTICS solar cell (SCC2422 model). Measurements were performed at light intensity of 800 Lux or less, corresponding to the indoor illuminance. Light intensity was adjusted by changing the distance between the designed chip and the lamp (light source). The open-circuit voltage of the PV cell at 700 Lux is approximately 1 V and the maximum available power is 17.3 μ W. The storage capacitor C_{STO} is set to 47 μ F.

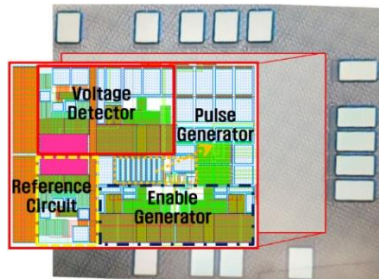


Figure 8. Layout and photograph of the designed MPPT interface circuit



Figure 9. Experimental setup for photovoltaic energy harvesting

Figure 10 shows the measurement results for photovoltaic energy harvesting. Figures 10(a) and (b) are the steady-state waveforms of the output voltage of the PV cell (V_{PV}), the MPPT pulse (MC), and the load voltage (V_{Load}) at 700 Lux when R_{Load} is 18 k Ω . It can be seen from Figure 10(a) that the MC signal is generated at a period of 2.5 seconds, and when the MC signal is high, SW1 is turned off, and the open-circuit voltage $V_{PV,OC}$ of about 1 V is generated. It can also be seen from Figure 10(b) that the output voltage of the PV cell is band-band controlled between 662 mV and 750 mV by the MPPT controller. Excluding the time during which $V_{PV,OC}$ occurs, the average voltage of V_{PV} (and hence V_{STO}) is 706 mV, which is slightly different from the MPP voltage of 700 mV (0.7 times $V_{PV,OC}$). Therefore, it can be confirmed that the PV cell operates in the vicinity of the MPP. The V_{Load} follows V_{PV} during the discharging phases, which correspond to the active time the load can operate. The operating duty cycle depends on the load resistance. It is 47.3% for R_{Load} =18 k Ω but increases to 72.8% for R_{Load} =25 k Ω shown in Figure 10(c). The current required by the load decreases as the load resistance increases. Therefore, the discharge rate decreases, and the duty cycle increases.

Figure 10(d) shows the waveforms measured when $V_{PV,OC}$ is decreased from 1 V to 250 mV at $t=t_1$ to verify the operating characteristics of the voltage detector addressed in section 2.4. When the light intensity decreases to a level where the energy harvesting operation is difficult (i.e. $V_{PV,OC}$ =250 mV), V_{PV} (and thus V_{STO}) cannot be boosted in the charging phase. Rather, it gradually decreases due to the discharge of C_{STO} by leakage current to the input terminal and to the MPPT control block. When V_{STO} decreases to the threshold value at $t=t_2$, the output VD of the voltage detector changes from '1' to '0', and the entire circuit is disabled. In this design, the threshold value is 250 mV, and it can be seen that the voltage detector detects at 240 mV by the hysteresis function.

Figure 11 shows the result of measuring the MPP tracking process when the light intensity changes. The load resistance is 18 k Ω . When the light intensity is changed from 800 Lux to 470 Lux (or vice versa), the open-circuit voltage $V_{PV,OC}$ changes from 1.26 V to 0.89 V (or vice versa). The average value of V_{PV} is 0.87 V for $V_{PV,OC}$ =1.26 V, and 0.62 V for $V_{PV,OC}$ =0.89 V. So, it can be seen that the designed circuit is able to track the MPP voltage even when there is a change in light intensity.

When the energy transducer's output changes, the transition time it takes to track a new MPP depends on the timing of the MC signal generation. The worst case is when the output of the energy transducer changes immediately after the n -th MC signal is generated. In this case, energy is harvested based on the $V_{MPP}[n\text{-th}]$ generated by the n -th MC signal until the $(n+1)$ -th MC signal is generated. Therefore, the maximum transition time is the time obtained by adding the period of the MC signal and the time to charge or discharge C_{STO} based on the updated $V_{MPP}[(n+1)\text{-th}]$. Figure 11(a) corresponds to this worst case, and the maximum transition time is 1.5 seconds. On the other hand, if the output of the energy transducer changes just before the $(n+1)$ -th MC signal is generated, the transition time becomes minimum and corresponds to the time to charge or discharge C_{STO} based on the updated $V_{MPP}[(n+1)\text{-th}]$. Figure 11(b) corresponds to this best case, and the minimum transition time is 0.4 seconds.

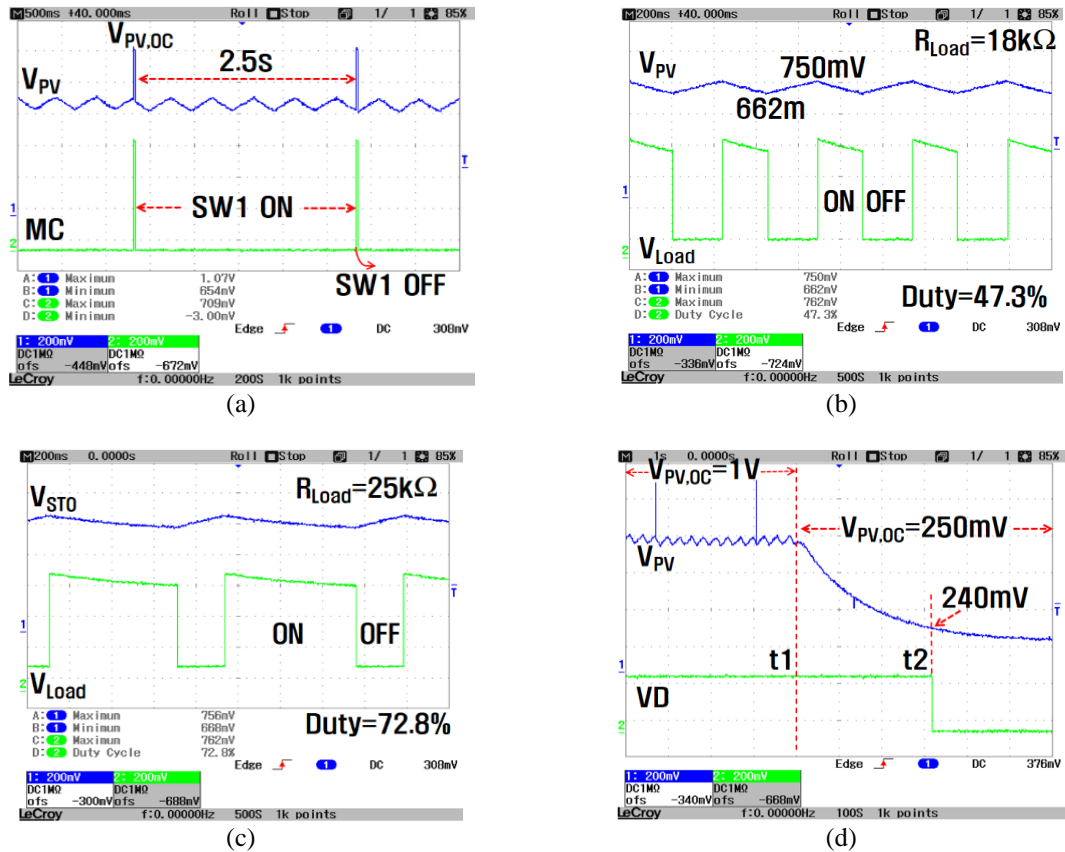


Figure 10. Waveforms measured for photovoltaic energy harvesting (a) V_{PV} and MC , (b) V_{PV} and V_{Load} when $V_{PV,OC} \approx 1$ V (700 Lux) and $R_{Load} = 18$ k Ω , (c) duty cycle change due to R_{Load} increase to 25 k Ω , and (d) waveforms measured when $V_{PV,OC}$ changes from 1 V to 250 mV to verify the voltage detector functionality

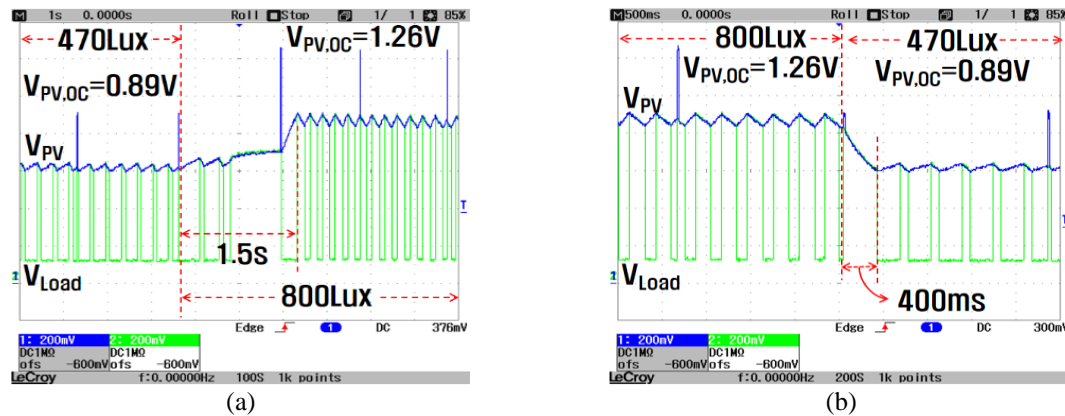


Figure 11. MPP tracking process, measured waveforms of V_{PV} and V_{Load} when the light intensity is changed (a) from 470 Lux to 800 Lux and (b) from 800 Lux to 470 Lux

3.2. Measurement results for thermal energy

A TEG can be emulated by a voltage source V_T connected in series with a resistor R_T [8]. For example, a 1-V DC voltage source with a 25-k Ω resistor can be used to emulate the TEG device presented in [32]. For the TEG emulation circuit, the open-circuit voltage is 1 V, and the maximum available power is 10 μ W. The storage capacitor C_{STO} is set to 47 μ F.

Figures 12(a) and (b) show the measurement results under the minimum operating voltage condition that the designed MPPT interface circuit can operate. They show the waveforms of V_{TEG} and V_{Load} when

$V_T=0.6$ V, $R_T=25$ k Ω , and $R_{Load}=10$ k Ω . In this case, the open-circuit voltage of the input device is 0.6 V, so the interface circuit should operate at the MPP voltage (ideally 0.3 V). It can be seen that V_{TEG} is between 281 mV and 303 mV, and the average voltage of V_{TEG} is 292 mV, which is close to the MPP voltage of 300 mV. This result demonstrates that the designed circuit can operate properly even at operating voltage as low as 0.3 V. The duty-cycle change with load resistance and the MPP tracking process for thermoelectric energy harvesting are similar to those for photovoltaic energy harvesting shown in Figures 10 and 11.

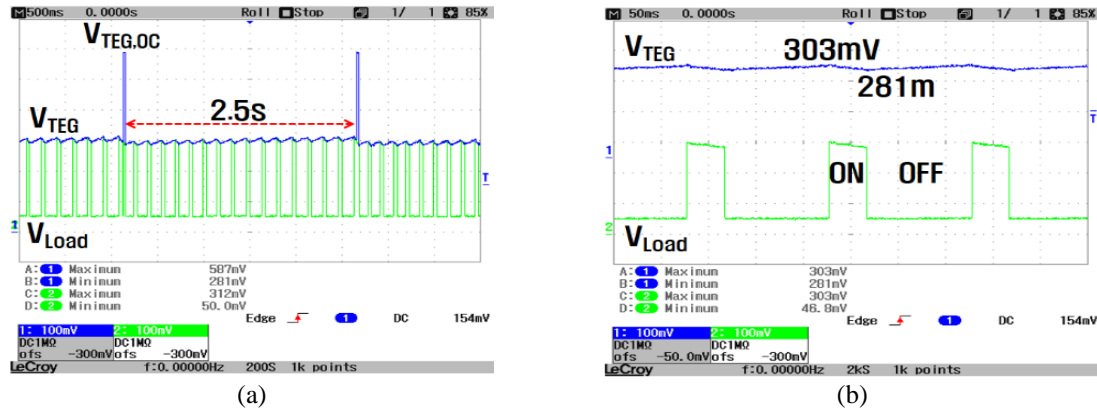


Figure 12. Measured waveforms for thermoelectric energy when $V_T=0.6$ V, $R_T=25$ k Ω , and $R_{Load}=10$ k Ω
(a) V_{TEG} and V_{Load} and (b) magnified view of V_{TEG} and V_{Load}

3.3. Power efficiency and MPPT accuracy

The power efficiency measured for different load resistances is shown in Figure 13(a). It is defined as the ratio of the power delivered to the load to the maximum available power of the transducer. Efficiency was measured using an equivalent circuit for the PV cell and a TEG emulation circuit with $V_T=1$ V and $R_T=25$ k Ω for the TEG. For the PV cell, the peak power efficiency is 97.1%, and the efficiencies are greater than 90% for $400 \Omega \leq R_{Load} \leq 5$ k Ω . The operating duty cycle becomes 100% for $R_{Load} > 5$ k Ω . Thus, the circuit operates in continuous mode and deviates from the MPP with reduced efficiency. As the load resistance decreases, the power efficiency decreases due to an increase in the current at the power switches SW1 and SW2 and the resulting increase in conduction losses. For the TEG, the peak power efficiency is 93.6%, and the efficiencies are greater than 80% for $15 \text{ k}\Omega \leq R_{Load} \leq 50$ k Ω . For $R_{Load} > 27$ k Ω , the duty cycle becomes 100%.

The MPP tracking accuracy of the designed circuit is shown in Figure 13(b). It is defined as the ratio of the output power generated by the energy transducer to the maximum available power of the transducer. In this measurement, $P_{PV,MAX}=117 \mu\text{W}$ and $P_{TEG,MAX}=10 \mu\text{W}$. The tracking accuracy for the PV cell is better than 98.3% in the R_{Load} range of less than 5 k Ω where the MPPT operation is maintained as the operating duty cycle is less than 100%. The tracking accuracy for the TEG is better than 98.8% in the R_{Load} range of less than 27 k Ω . It shows satisfactory performance of the proposed MPPT interface circuit. Table 2 compares the performance of conventional low-voltage DC-type energy harvesting circuits with the presented circuit. Since the proposed circuit shows high MPPT accuracy and occupies a relatively small area, it is suitable for low-voltage low-power sensor application systems that does not require start-up circuits.

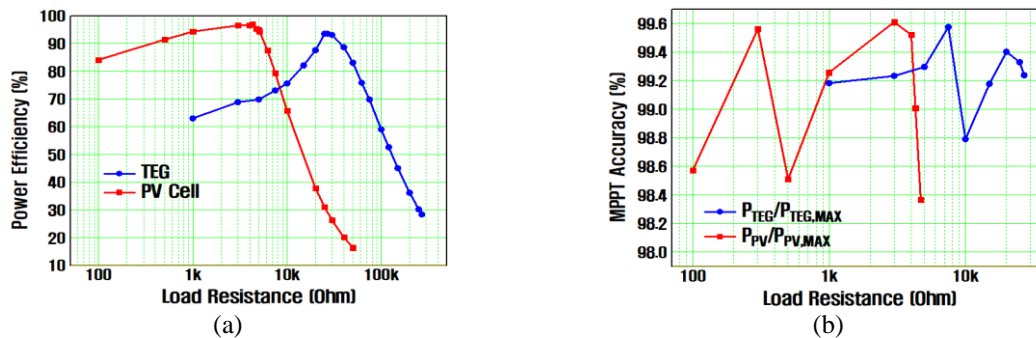


Figure 13. Performance of the designed MPPT interface circuit (a) power efficiency and (b) MPP tracking accuracy

Table 2. Performance comparison with conventional low-voltage DC-type energy harvesting circuits

Parameter	[4]	[17]	[21]	[33]	[34]	This work
Process	0.18 μm	0.18 μm	65 nm	0.32 μm	0.18 μm	65 nm
Type of sources	PV	DC	TEG	DC	TEG	DC
Input voltage (V _{oc})	0.14~0.62 V	30 mV~1.8 V	80 mV~	74 mV~2.5 V	60 mV~0.46 V	0.6~1.2 V
V _{out} (V) [*: regulated]	*1.0	3~5.8	1.3	*1.8	*1~1.8	0.3~0.84
Requirement for startup	Charge pump	Pre-charged battery	V _{TH} -tuned OSC & charge pump	Charge pump	Charge pump	None
DC-DC conversion	Inductive boost	Inductive buck-boost	Inductive boost	Inductive boost	Inductive boost	None
MPPT scheme	None	FOCV	None	FOCV	None	FOCV
Peak efficiency (%)	82	90.2	60 (just BC)	77.1	78.5	97.1
Current/power [*: quiescent]	*3.2 nW	N/A	N/A	*121 nA	8.2 μW	130 nW @ 1 V
Active area (mm ²)	2.42	2.58	0.25	0.93	0.53	0.43

4. CONCLUSION

This paper presented a simple implementation of an MPPT interface circuit for low-voltage DC-type energy harvesting sources. The interface circuit is driven directly by the low output voltages of small size energy transducers, eliminating the need for complex start-up circuitry. A simple MPPT controller with the FOCV method was presented and fabricated in a 65-nm CMOS process. The designed chip occupies an active area of 720 μm ×640 μm and consumes 130 nW for an open-circuit voltage of 1 V. It has been experimentally verified that the designed MPPT interface can track the MPP voltage even in the presence of fluctuations in the open-circuit voltage and can operate properly at operating voltages as low as 0.3 V. The proposed circuit can be applied to energy transducers with lower output voltages if finer and more advanced processes are used. The measured peak power efficiency is 97.1%, and the MPP tracking accuracy is better than 98.3%. The proposed circuit is suitable for self-powered small size sensor systems because it does not require a start-up circuit or even dc-dc boost converters.

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REFERENCES

- [1] T. Ruan, Z. J. Chew and M. Zhu, "Energy-Aware Approaches for Energy Harvesting Powered Wireless Sensor Nodes," *IEEE Sensors Journal*, vol. 17, no. 7, pp. 2165-2173, April 2017, doi: 10.1109/JSEN.2017.2665680.
- [2] M. J. Weber, Y. Yoshihara, A. Sawaby, J. Charthad, T. C. Chang and A. Arbabian, "A Miniaturized Single-Transducer Implantable Pressure Sensor With Time-Multiplexed Ultrasonic Data and Power Links," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 4, pp. 1089-1101, April 2018, doi: 10.1109/JSSC.2017.2782086.
- [3] E. Dallago, A. L. Barnabei, A. Liberale, P. Malcovati and G. Venchi, "An Interface Circuit for Low-Voltage Low-Current Energy Harvesting Systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1411-1420, March 2015, doi: 10.1109/TPEL.2014.2322521.
- [4] D. E.-Damak and A. P. Chandrakasan, "A 10 nW–1 μW Power Management IC With Integrated Battery Management and Self-Startup for Energy Harvesting Applications," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 943-954, April 2016, doi: 10.1109/JSSC.2015.2503350.
- [5] B. Yu and S. -C. Ko, "Power dissipation analysis of PV module under partial shading," *International Journal of Electrical and Computer Engineering*, vol. 11, no. 2, pp. 1029-1035, April 2021, doi: 10.11591/ijece.v11i2.pp1029-1035.
- [6] C. Lu, C. -Y. Tsui and W. -H. Ki, "Vibration Energy Scavenging System With Maximum Power Tracking for Micropower Applications," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 11, pp. 2109-2119, Nov. 2011, doi: 10.1109/TVLSI.2010.2069574.
- [7] X. Wang *et al.*, "Multi-Input SECE Based on Buck Structure for Piezoelectric Energy Harvesting," in *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3638-3642, April 2021, doi: 10.1109/TPEL.2020.3022424.
- [8] Y. K. Ramadass and A. P. Chandrakasan, "A Battery-Less Thermoelectric Energy Harvesting Interface Circuit With 35 mV Startup Voltage," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 333-341, Jan. 2011, doi: 10.1109/JSSC.2010.2074090.
- [9] E. -J. Yoon, J.-T. Park and C.-G. Yu, "Thermal energy harvesting circuit with maximum power point tracking control for self-powered sensor node applications," *Frontiers of Information Technology & Electronic Engineering*, vol. 19, pp. 285–296, 2018, doi: 10.1631/FITEE.1601181.
- [10] P. Li, Z. Long and Z. Yang, "RF Energy Harvesting for Batteryless and Maintenance-Free Condition Monitoring of Railway Tracks," in *IEEE Internet of Things Journal*, vol. 8, no. 5, pp. 3512-3523, 1 March 2021, doi: 10.1109/JIOT.2020.3023475.
- [11] E. J. Yun, H. J. Kim and C. G. Yu, "A multi-input energy harvesting system with independent energy harvesting block and power




- management block," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 24, no. 3, pp. 1379-1391, Dec. 2021, doi: 10.11591/ijeecs.v24.i3.pp1379-1391.
- [12] D. Selvaraj and D. Rangasamy, "Electric vehicle charging using roof top photovoltaic controlled with new hybrid optimization technique," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 26, no. 3, pp. 1227-1234, June 2022, doi: 10.11591/ijeecs.v26.i3.pp1227-1234.
- [13] A. Ibelouad, A. Elkari, H. Ayad and M. Mjahed, "A neuro-fuzzy approach for tracking maximum power point of photovoltaic solar system," *International Journal of Power Electronics and Drive Systems*, vol. 12, no. 2, pp. 1252-1264, June 2021, doi: 10.11591/ijpeds.v12.i2.pp1252-1264.
- [14] M. Atig, Y. Miloud, A. Miloudi and A. Merah, "A novel optimization of the particle swarm based maximum power point tracking for photovoltaic systems under partially shaded conditions," *International Journal of Power Electronics and Drive Systems*, vol. 12, no. 3, pp. 1795-1803, Sept. 2021, doi: 10.11591/ijpeds.v12.i3.pp1795-1803.
- [15] R. J. M. Vullers, R. V. Schaijk, I. Doms, C. V. Hoof and R. Mertens, "Micropower energy harvesting," *Solid-State Electronics*, vol. 53, no. 7, pp. 684-693, July 2009, doi: 10.1016/j.sse.2008.12.011.
- [16] D. Dondi, A. Bertacchini, D. Brunelli, L. Larcher and L. Benini, "Modeling and Optimization of a Solar Energy Harvester System for Self-Powered Wireless Sensor Networks," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2759-2766, July 2008, doi: 10.1109/TIE.2008.924449.
- [17] E.-J. Yoon and C.-G. Yu, "Power management circuits for self-powered systems based on micro-scale solar energy harvesting," *International Journal of Electronics*, vol. 103, no. 3, pp. 516-529, 2016, doi: 10.1080/00207217.2015.1036802.
- [18] H. Kim, J. Maeng, I. Park, J. Jeon, D. Lim and C. Kim, "A 90.2% Peak Efficiency Multi-Input Single-Inductor Multi-Output Energy Harvesting Interface With Double-Conversion Rejection Technique and Buck-Based Dual-Conversion Mode," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 3, pp. 961-971, March 2021, doi: 10.1109/JSSC.2020.3025722.
- [19] Y. -K. Teh and P. K. T. Mok, "Design of Transformer-Based Boost Converter for High Internal Resistance Energy Harvesting Sources With 21 mV Self-Startup Voltage and 74% Power Efficiency," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2694-2704, Nov. 2014, doi: 10.1109/JSSC.2014.2354645.
- [20] B. -M. Lim, J. -I. Seo and S. -G. Lee, "A Colpitts Oscillator-Based Self-Starting Boost Converter for Thermoelectric Energy Harvesting With 40-mV Startup Voltage and 75% Maximum Efficiency," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3293-3302, Nov. 2018, doi: 10.1109/JSSC.2018.2863951.
- [21] P. -H. Chen *et al.*, "A 80-mV input, fast startup dual-mode boost converter with charge-pumped pulse generator for energy harvesting," *IEEE Asian Solid-State Circuits Conference 2011*, 2011, pp. 33-36, doi: 10.1109/ASSCC.2011.6123562.
- [22] M. Rakús, V. Stopjaková and D. Arbet, "Design techniques for low-voltage analog integrated circuits," *Journal of Electrical Engineering*, vol. 68, pp. 245-255, 2017, doi: 10.1515/jee-2017-0036.
- [23] H. Shao, C. -Y. Tsui and W. -H. Ki, "The Design of a Micro Power Management System for Applications Using Photovoltaic Cells With the Maximum Output Power Control," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 8, pp. 1138-1142, Aug. 2009, doi: 10.1109/TVLSI.2008.2001083.
- [24] L. H. C. Ferreira, T. C. Pimenta and R. L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 843-847, Oct. 2007, doi: 10.1109/TCSII.2007.902216.
- [25] B. J. Blalock, P. E. Allen and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," in *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 7, pp. 769-780, July 1998, doi: 10.1109/82.700924.
- [26] B. S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," in *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 634-643, Dec. 1983, doi: 10.1109/JSSC.1983.1052013.
- [27] C. Galup-Montoro, M. C. Schneider and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," in *IEEE Journal of Solid-State Circuits*, vol. 29, no. 9, pp. 1094-1101, Sept. 1994, doi: 10.1109/4.309905.
- [28] S. Chakraborty, A. Mallik, C. K. Sarkar and V. Ramgopal Rao, "Impact of Halo Doping on the Subthreshold Performance of Deep-Submicrometer CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications," in *IEEE Transactions on Electron Devices*, vol. 54, no. 2, pp. 241-248, Feb. 2007, doi: 10.1109/TED.2006.888630.
- [29] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1609-1617, June 2014, doi: 10.1109/TCSI.2013.2289413.
- [30] R. J. Baker, "Current Mirrors," in *CMOS Circuit Design, Layout, and Simulation*, 4th ed. Piscataway, NJ, USA: Wiley, pp. 633-638, 2019.
- [31] W. Li, R. Yao and L. Guo, "A low power CMOS bandgap voltage reference with enhanced power supply rejection," *2009 IEEE 8th International Conference on ASIC*, 2009, pp. 300-304, doi: 10.1109/ASICON.2009.5351450.
- [32] V. Leonov, P. Fiorini, S. Sedky, T. Torfs and C. Van Hoof, "Thermoelectric MEMS generators as a power supply for a body area network," *The 13th International Conference on Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05.*, 2005, pp. 291-294 Vol. 1, doi: 10.1109/SENSOR.2005.1496414.
- [33] M. Dini, A. Romani, M. Filippi and M. Tartagni, "A Nanocurrent Power Management IC for Low-Voltage Energy Harvesting Sources," in *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4292-4304, June 2016, doi: 10.1109/TPEL.2015.2472480.
- [34] J. -J. Jhang, H. -H. Wu, T. Hsu and C. -L. Wei, "Design of a Boost DC-DC Converter With 82-mV Startup Voltage and Fully Built-in Startup Circuits for Harvesting Thermoelectric Energy," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 54-57, 2020, doi: 10.1109/LSSC.2020.2978850.

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