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MITA interleaver for OFDM-IDMA and SCFDMA-IDMA techniques using QPSK modulation over PLC

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ABSTRACT

The paper aims to examine the performance of multiplicative interleaving with tree algorithm (MITA) interleaver for grouped IDMA systems i.e., SCFDMA-IDMA and OFDM-IDMA, using QPSK modulation over powerline channel. The prime objective is to evaluate the MITA algorithm for its complexity and throughput over multiple communication systems so that it fulfills the requirements of 5G technology. Higher throughput and low complexity are achieved by the structure of MITA interleaver, in which more users are allotted interleavers per clock cycle as compared to existing interleavers primarily, random, tree, and FLRITI. The analysis is carried out in MATLAB environment for varying parameter values such as data length and user count and is plotted in terms of bit error rate (BER). Next, the effect of Convolutional coding is observed on grouped IDMA systems and lastly comparison in terms complexity is carried out. The simulation results over grouped IDMA systems show that MITA interleaver has better BER performance than FLRITI for large user count and the response further improves with greater number of users. The comparison of interleavers in terms of complexity reveals that MITA has lower complexity than FLRITI. Thus, MITA interleaver can be preferred over FLRITI and is a better option to be implemented in 5G technologies.

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1. INTRODUCTION

The fifth generation (5G) technology aims to provide reliable communication with high throughput and low latency to vast number of mobile users and home automated devices [1], [2]. One approach could be the use of powerline channel for reliable communication with higher throughput as most smart devices in home network are non-portable [3], [4]. A major drawback in the stated method is that the powerlines were not designed for communication and it poses hurdle in the path of the signals. The primary disturbances in powerline channel comprises of burst impulsive noise, frequency selective fading and multi access interference [5], [6]. These obstacles can be nullified by the application of multiple access technique. Interleave division multiple access (IDMA) scheme can effectively negate the impact of burst impulsive noise by the interleaving mechanism [7]. Orthogonal frequency division multiple access (OFDMA) technique can suppress the interference in channel and single carrier frequency division multiple access (SCFDMA) technique aids in reducing the effect of fading [8]. However, as the burst impulsive noise has the most significant impact on reliability of powerline communication, IDMA is integrated with either OFDM or SCFDMA technique.

IDMA scheme is a derivative of code division multiple access (CDMA) technique and inherits the advantages of CDMA with a significant difference in the system architecture [9], [10]. IDMA scheme employs interleaving as a sole mechanism to distinguish users in the medium whereas CDMA uses user-specific spreading codes. Interleaving is the mechanism of randomly arranging the data bits at the transmitter and rearranging at the receiver, thus distributing the error bits in the received signal throughout the span of signal. Interleavers also play a pivotal role in the 5G communication and serves as one foundation of code domain NOMA technique [11], [12], thus to find an optimal interleaver in terms of latency and throughput is the need of the hour.

In literature various interleavers have been proposed [13]-[20], for instance random, tree, FLRITI, MITA which have been assessed over parameters such as memory requirement, computation complexity and bit error rate (BER) over wireless channels and recently over PLC. The random interleaver (RI) was implemented over powerline in [15] over conventional IDMA system and was evaluated using MATLAB environment. The simplicity of generation and execution made RI quite popular but the vast memory requirement restricted its use. The tree interleaver (TI) proposed by Shukla *et al.* [16]. TI possesses the advantage of reduced memory requirement in comparison to RI with same BER performance and thus gained importance quite rapidly. A derived version of TI, flip left- right approach based inverse tree interleaver (FLRITI) was simulated over wireless channel in [17], [18], sometime referred as inverse tree interleaver, further downsized the memory requirement for same performance and have been implemented over powerline in [19]. Recently, multiplicative interleaving with tree algorithm (MITA) interleaver proposed in [20], was compared and simulated over powerline channel. The distinguishable feature of MITA interleaver is the reduced computational complexity for same memory and BER performance as of TI.

From the literature it can be inferred that the performance of MITA interleaver has been judged for IDMA and OFDM-IDMA scheme using BPSK modulation over powerline channel but rarely assessed over SCFDMA-IDMA system, as per author's knowledge. Secondly, the estimation of interleaver behavior has not been thoroughly analyzed over Quadrature phase shift keying (QPSK) modulation technique. Thus, the motive of the paper is to carry out the performance analysis of MITA interleaver over grouped IDMA systems, i.e., OFDM-IDMA and SCFDMA-IDMA for QPSK modulation over powerline channel. Next, the comparison of MITA interleaver has been carried out against random, tree and FLRITI for uncoded and coded systems in terms of bit error rate (BER) and computation complexity. Lastly, MITA interleaver has been compared with FLRITI for varying user count over SCFDMA-IDMA system. The layout of the paper is as follows: section 2 explains the functionality of MITA interleaver. Section 3 describes the grouped IDMA systems i.e., OFDM-IDMA and SCFDMA-IDMA systems. The performance analysis of grouped IDMA systems for various parameter values is assessed in section 4 and finally the conclusion is presented in section 5.

2. THE PROPOSED ALGORITHM

Recently proposed MITA interleaver [20], shown in Figure 1, promised reduced computation complexity without any extra expense on bit error rate. It is derived from tree interleaver proposed by Shukla in [16] but possess some significant modifications in the structure and principle of generation of interleavers. The sole similarity is that both the structures grow from 2 main nodes i.e., there are 2 users in the first stage which have orthogonal interleaving sequences π1 and π2, also referred as master random interleavers. In MITA interleaver the number of users in each stage is represented as $NU_S=3NU_{S-1}-1$, where S is the stage number and its starting value is 2 and in tree interleaver users are computed as $NU_S=2^S$. Thus, the user count in MITA progresses as {5, 14, 41…} whereas for TI users in each stage are {4, 8, 16, 32…}, therefore as stage number increases user count per stage is greater in MITA in comparison to Tree interleaver. Secondly, in MITA interleaver users are allocated branch in order of their channel access as opposed to even and odd assignment of branches in Tree interleaver. Next, the interleaver generation for further users in TI is a combination of master interleavers π1 and π2, however in MITA interleaver reciprocity concept is also put to use 2nd stage onwards. The principle of interleaver generation using MITA algorithm is:

a. Generate the two master random interleavers л1, л2 and allot it to User 1 and 2 respectively.
b. Compute the number of stages using formula: $NU_S=3NU_{S-1}-1$, where S is the stage number.
c. If the user count in a stage less than $3NU_{s-1}$, then master random interleaver л1 is required to produce further interleavers else master random interleaver л2 is approached.
d. For instance, interleaving sequences for user numbers 3-5 are computed as: p3=(л1(л1))=(л1)2, p4=(л1(л1))-1=((л1)2)-1, p5=(л1(л2)) and for users 6,7 (greater than $3NU_{s-1}$): p6=(л2(л2))=(л2)2, p7=(л2(л2))-1=((л2)2)-1.
e. The steps three and four are reiterated if stage is greater than 2.

The flowchart of the MITA interleaver algorithm is depicted in Figure 2. The interleaving pattern generation for multiple users is illustrated in Table 1.

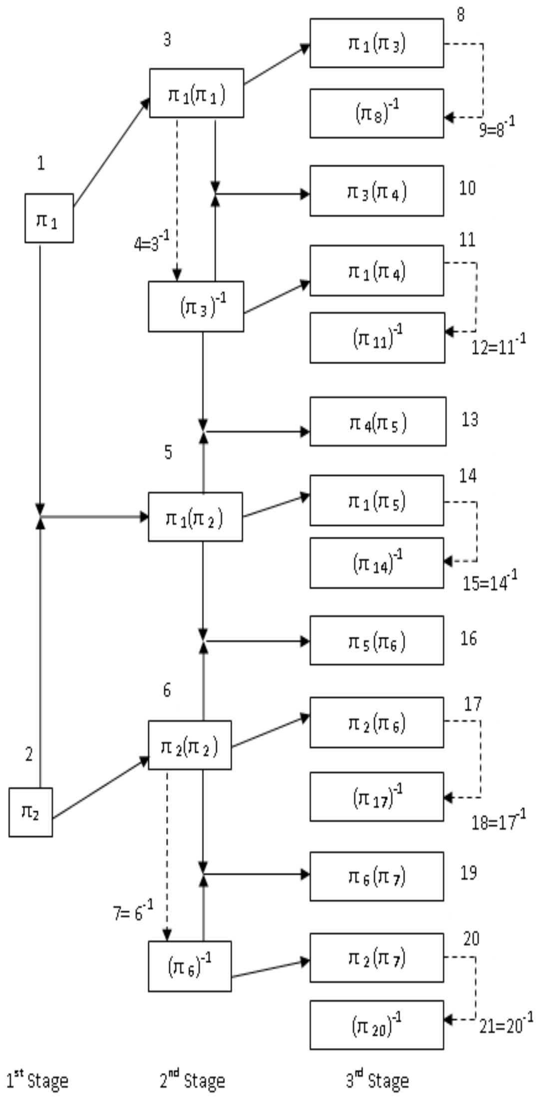


Figure 1. Structure of MITA interleaver for 3 stages

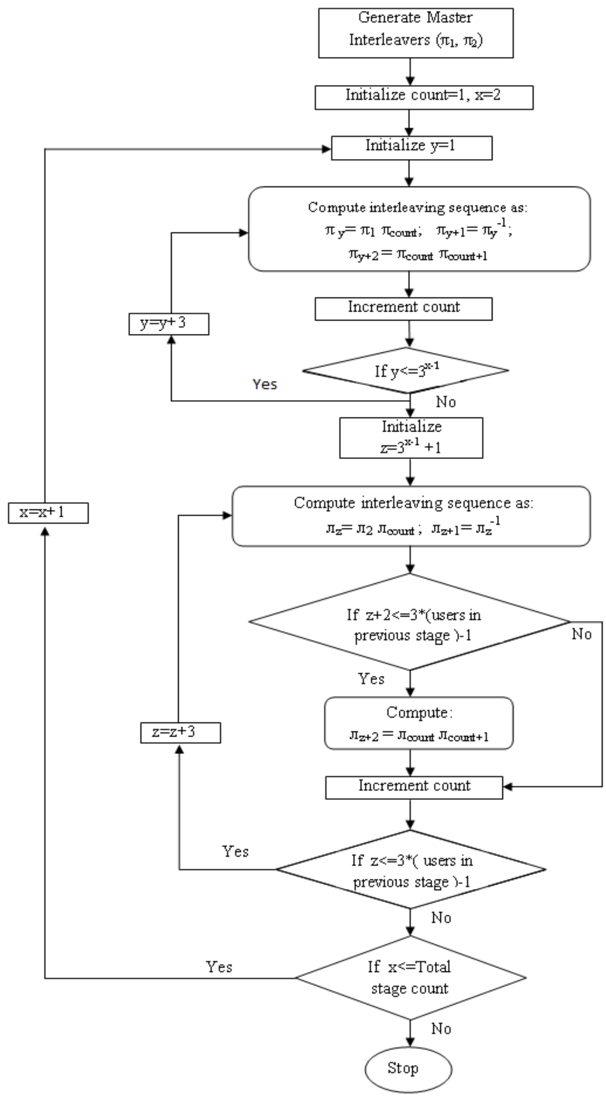


Figure 2. Flowchart of algorithm of MITA interleaver

Table 1. Interleaving patterns of 20 users using MITA interleaver

User	Interleaver	User	Interleaver
1	$p_{1=}л_1$	11	$p_{11}=p_1*p_4=(л_1(л_1(л_1))^{-1})$
2	$p_{2=}л_2$	12	$p_{12}=p_{11}^{-1=}(л_1(л_1(л_1))^{-1})^{-1}$
3	$p_{3=}p_1^{2=}(л_1(л_1))$	13	$p_{13}=p_4*p_{5=}(((л_1(л_1))^{-1}\ (л_1(л_2)))$
4	$p_{4=}p_3^{-1=}(л_1(л_1))^{-1}$	14	$p_{14}=p_1*\ p_5=(л_1(л_1(л_2)))$
5	$p_5=p_1*p_{2=}(л_1(л_2))$	15	$p_{15=}p_{14}^{-1=}(л_1(л_1(л_2)))^{-1}$
6	$p_{6=}p_2^2=(л_2(л_2))$	16	$p_{16}=p_5*p_{6=}((л_1(л_2))\ (л_2(л_2)))$
7	$p_{7=}p_6^{-1=}(л_2(л_2))^{-1}$	17	$p_{17}=p_2*p_6=(л_2(л_2(л_2)))$
8	$p_8=p_1^3=(л_1(л_1(л_1)))$	18	$p_{18=}p_{17}^{-1}=(л_2(л_2(л_2)))^{-1}$
9	$p_{9=}p_8^{-1}=(л_1(л_1(л_1)))^{-1}$	19	$p_{19}=p_6*p_7=((л_2(л_2))\ (л_2(л_2))^{-1})$
10	$p_{10}=p_3*p_{4=}(л_1(л_1(л_1(л_1))^{-1}))$	20	$p_{20}=p_2*p_{7=}(л_2(л_2(л_2))^{-1})$

The primary benefit of MITA interleaver is the reduction in computation complexity that is the outcome of structural modifications as compared to Tree interleaver. Computation complexity is explained as the total clock cycles required for generation of interleaving patterns for defined users in a system. As MITA interleaver has higher user count per stage, clock cycles required are less and the difference in clock cycle further reduces with increase in user count. This is a salient advantage as IDMA receiver incorporates Turbo processor which reiterates for specified number of times and aids in boosting the complexity of the system, thus an interleaver having reduced computations is a boon to IDMA scheme.

3. METHOD

The traditional IDMA system can improve quality of communication over powerline by combating the disturbance caused by burst impulse noise but lacks in removing the interference and fading effects of channel. Thus, the need for superior performance motivates for grouping of OFDM and SCFDMA techniques with IDMA scheme, i.e., OFDM-IDMA [21], [22], SCFDMA-IDMA [23], [24], which are competent in negating the outcomes of interference and fading. OFDM and SCFDMA are proficient in terms of performance and ease of implementation but have slightly different system model [25], [26]. OFDM ensures orthogonality of carriers for alleviating the effects of inter-carrier interference (ICI), inter-symbol interference (ISI) and frequency selective fading, whereas SCFDMA employs additional DFT in OFDM architecture to mitigate multipath propagation. Additionally, SCFDMA has less severe problems of peak to average power ratio (PAPR) than OFDM.

3.1. Description of OFDM-IDMA and SCFDMA-IDMA communication system

The block diagram of communication system of OFDM-IDMA and SCFDMA-IDMA are demonstrated in Figures 1-2. The grouped system can be addressed as non-traditional as the two techniques OFDM and SCFDMA were designed to work solely as a multiplexer/modulator. The IDMA scheme employed here is iterative IDMA as the receiver has a feedback loop, referred as Turbo Processor, which repeats for a specific number of times before producing a hard output [27].

3.1.1. OFDM-IDMA system

Figure 3 depicts the system flow only for a kth user, for simplicity, which can be expanded for K users, where the transmitter section consists of an encoder, spreader, interleaver and sub-carrier mapper (SCM) and OFDM modulator. The input data D_k is encoded by Convolutional coder [28] having memory as 2 and rate as ½, followed by spreading operation which has a length *sl* that results in bandwidth expansion and the produced data is commonly called as chips C_k. These two blocks are identical for all users and the differentiation among users is provided by the next step i.e., interleaver (π_k). The interleaver is user specific and randomizes the data so as to provide robustness against burst error.

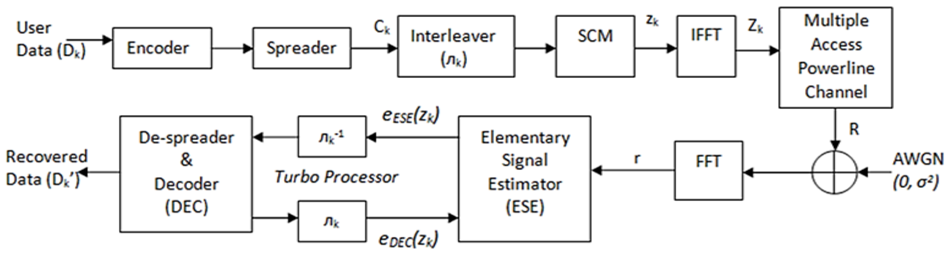


Figure 3. System representation of OFDM-IDMA technique

Next, the data is mapped according to QPSK modulation before performing the inverse fast Fourier transform (IFFT). The signal z_k is the collective representation of real and imaginary parts of signal and is expressed as: $z_k = z_k^{Re} + iz_k^{Im}$ after QPSK mapping, where Re and Im superscripts denote real and imaginary components. The IFFT yields signal *Z* such that: $Z_k = \frac{1}{N}\sum_{n=0}^{N-1} z_k e^{-2\pi ikn/N}$, where *N* is the number of subcarriers. The resultant signal is transmitted over multiple access powerline channels which is assumed to be influenced by Additive White Gaussian Noise (AWGN) having μ=0 and σ^2 variance. The received signal denoted by 'R' in elementary form is represented as: $R(k) = \sum_k Ɏ_k Z_k + \eta$, where $Ɏ_k$is the channel coefficient ($Ɏ_k = Ɏ_k^{Re} + iɎ_k^{Im}$) and η accounts for the noise and interference in the channel. The definitive form of complex received signal is given as:

$$R(n) = \sum_k\left(Ɏ_k^{Re} Z_k^{Re}(n) - Ɏ_k^{Im} Z_k^{Im}(n)\right) + i\sum_k\left(Ɏ_k^{Re} Z_k^{Im}(n) - Ɏ_k^{Im} Z_k^{Re}(n)\right) + \eta(n) \quad (1)$$

The received signal is transformed to frequency domain via FFT before feeding to IDMA receiver, that follows chip by chip (CBC) detection and the received signal of user k on a particular subcarrier *n* is written in composite form as:

$$r(n) = \sum_{k'=1}^{K} ɏ_{k'}(n) z_{k'}(n) + \eta(n) = y_k(n) z_k(n) + \xi(n) \quad (2)$$

where, y_k is the channel coefficient after FFT transform and $\xi(n)$ accounts for the disturbances faced by k^{th} user at n^{th} subcarrier and is derived as: $\xi(n)=\sum_{k\neq k'} \mathrm{y}_k(n) z_k(n) + \eta(n)$. The IDMA receiver [27], [28], Turbo Processor, comprises of Elementary Signal Estimator (ESE), duo of interleaving (π) and de-interleaving (π^{-1}) process and finally de-spreader and decoder block (DEC). The working of Turbo processor is pointed out only for Real part of the signal and the same steps are replicated for Imaginary part. The function of ESE is to generate a rough estimate on the bit value by computing the mean and variance of signal and interference as:

$$E\left(r^{Re}(n)\right) = \sum_k \left(\mathrm{y}_k^{Re} E\left(z_k^{Re}(n)\right) - \mathrm{y}_k^{Im} E\left(z_k^{Im}(n)\right)\right) \tag{3}$$

$$Var\left(r^{Re}(n)\right) = \sum_k |\mathrm{y}_k^{Re}|^2 Var\left(z_k^{Re}(n)\right) + \sum_k |\mathrm{y}_k^{Im}|^2 Var\left(z_k^{Im}(n)\right) + \sigma^2 \tag{4}$$

The output of ESE block e_{ESE} is de-interleaved, de-spread, decoded and an estimate of the original bit is produced e_{DEC}. The generated output is interleaved and fed back to ESE block. The estimate of ESE and DEC blocks is generated as log likelihood ratios (LLR's) of the fed signal (f) and is expressed as:

$$e_{LLR}\left(z_k^{Re}(n)\right) = \log\left(\frac{p(f/z_k^{Re}(n)=+1)}{p(f/z_k^{Re}(n)=-1)}\right), \forall\ k, n \tag{5}$$

For generating e_{ESE}, the input to the ESE block is substituted in (5) to get the output of ESE block which is further de-interleaved to be processed by DEC block.

$$e_{ESE}\left(z_k^{Re}(n)\right) = 2\mathrm{y}_k^{Re} \frac{r^{Re}(n) - E\left(\xi^{Re}(n)\right)}{Var\left(\xi^{Re}(n)\right)} \tag{6}$$

The DEC operates on the principle of a posteriori probability (APP) algorithm and generates the estimate of input bit. The e_{DEC} is finally employed to update the statistical parameters mean and variance of the transmitted signal. The assessment of bit value by DEC is a soft decision and a hard decision is generated only after specific number of times. The aforementioned steps are reiterated for the imaginary bit of the signal.

3.1.2. SCFDMA-IDMA system

The block diagram of SCFDMA-IDMA is represented by Figure 4. The structure is almost same as OFDM-IDMA with an additional DFT-IDFT pair. In SCFDMA technique different subcarriers are allotted to different users which spread the data over the entire assigned bandwidth and also facilitate multiple access. The mathematical modeling of SCFDMA-IDMA system is a replica of OFDM-IDMA hence it is not discussed again and the same can be consulted from [23].

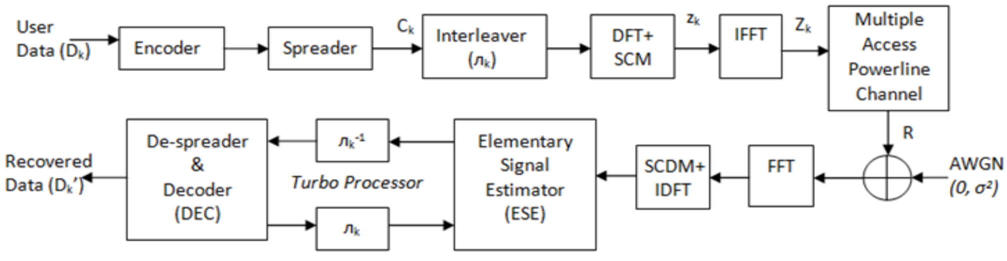


Figure 4. Block diagram of SCFDMA-IDMA system

3.2. Powerline channel (PLC)

Powerline communication has gained importance rapidly as it provides an alternative to the wireless network connection without any extra hardware costs [29]. The modeling of powerline was intensive as it was not designed to propagate communication signals. However, Tonello and Versolatto [30] pursued transmission line principles in modeling the powerline channel, named as bottom-up approach, and the channel function by employing ABCD matrix. The basic electrical parameters of transmission line rely on the frequency of the broadband signal for the computation of its value. These parameters aid in determining the propagation constant (ϒ) and characteristic impedance (Z_o) of the transmission line which further aids in estimating the A, B, C, D parameters and the relation is given as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma L) & Z_o \sinh(\gamma L) \\ \frac{1}{Z_o}\sinh(\gamma L) & \cosh(\gamma L) \end{bmatrix} \quad (7)$$

where, L is the length of the transmission line in consideration. The A, B, C, D parameters computed by (7) assists in determining the transfer function of powerline as depicted in Figure 5. The interdependency is given as $\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$ [30], [31] and the transfer function can be formulated as:

$$Ɏ = \frac{V_2}{V_1} = \frac{Z_O}{AZ_O + B + CZ_O Z_S + DZ_S} \quad (8)$$

The below approach is straightforward and leads to a simplified expression of channel transfer function which is relatively easy to implement.

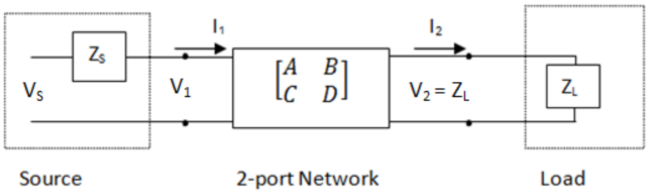


Figure 5. Modeling of transfer function of powerline channel

4. RESULTS AND DISCUSSIONS

The performance analysis of grouped IDMA system using QPSK modulation was carried out over MATLAB environment. The performance of MITA interleaver is compared against tree, FLRITI, and random interleavers. The systems were evaluated for both uncoded and coded systems for better understanding of the behavior of MITA interleaver. The simulations were performed for 16 users having data length as 512 bits and spreading length as 16, thus the resulting chip length is 8192 bits. The data is assumed to have 10 blocks and the iteration count of IDMA receiver was taken as 10. The channel employed was powerline channel having AWG noise so as to focus on the behavior of interleavers and the channel parameters used were:

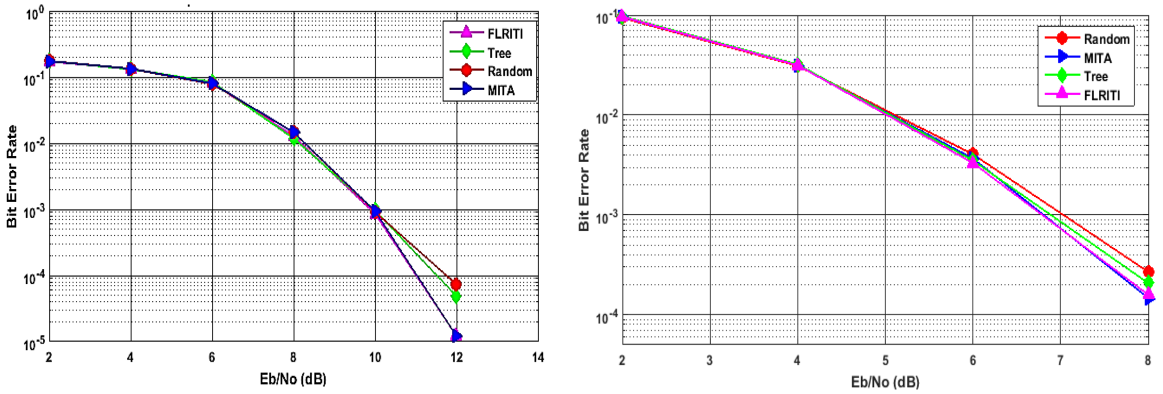
Table 2. Powerline channel simulation parameter values

Parameters	Values
freq	100 kHz
μ_0	4лx10^{-7} H/m
ε_0	8.85x10^{-12} F/m
ε_r	3.6
conductivity	5.8x10^{7} S/m
radius	1.12x10^{-3} m

4.1. Uncoded grouped systems

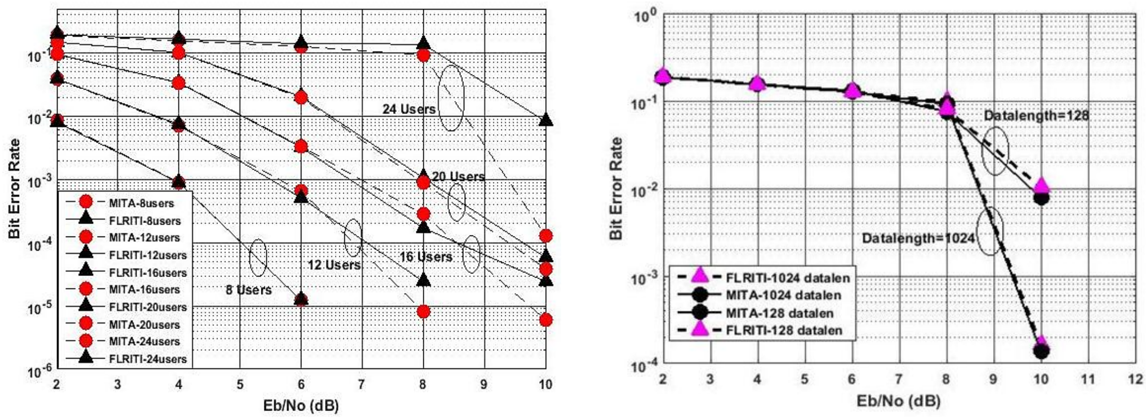
Firstly, the performance of interleavers is compared in the absence of coding. The simulation result of grouped IDMA system without coding is demonstrated in Figures 6(a)-(b) respectively. On observing the graphs, it can be deduced that the performance of MITA and FLRITI are better than tree and random interleavers for both integrated systems. Initially, the performance of all interleavers is same but with increase in bit energy the performance of MITA improves significantly, as greater the bit energy more is the probability of successful decoding and this also explains the sudden disappearance of graph. However, the performance of SCFDMA-IDMA system is better than OFDM-IDMA as the former requires lesser power for transmission of bits and thus is prone to lesser errors.

Next, comparison of MITA interleaver and FLRITI for varying user count and data length over SCFDMA-IDMA system is presented in Figures 7(a)-(b) respectively. The parameters taken for the simulation were: iterations=10, blocks=20 and data length=512bits. From the Figure 7(a), it can be observed that for fewer users the BER performance is almost identical but as the user count increases the performance of MITA is better than FLRITI. As noted from Figure 7(b), the BER performance of both interleavers is almost same and thus it can be concluded that size of data has less impact on the choice of interleaver.



(a) (b)

Figure 6. BER vs Eb/No of uncoded grouped IDMA system for multiple interleavers over PLC (a) OFDM-IDMA system and (b) SCFDMA-IDMA system



(a) (b)

Figure 7. Comparison of BER performance of MITA and FLRITI interleaver over SCFDMA-IDMA system (a) variation in user count and (b) variation in data length

Figure 8 demonstrates the effect of varying data length on the performance of MITA interleaver over grouped system for user count=24, blocks=10 and iteration count=10. As observed from the graph, the BER performance improves as data length increases for both systems. The improvement is due to the formation of greater number of orthogonal interleavers with increase in data length.

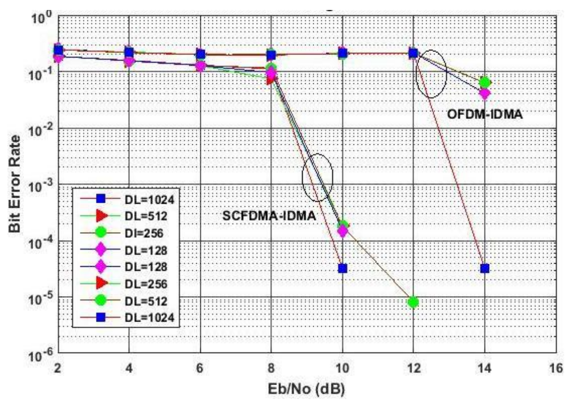


Figure 8. Variation of data length for grouped IDMA systems using MITA interleaver

4.2. Coded grouped systems

In this section the performance of interleavers is analyzed using forward error correction (FEC) technique Convolutional Coding having rate as ½ and memory 2. Coding aids in reducing the error in the system but increments the hardware complexity of the system, thus there is a trade-off. BER comparison of coded and uncoded grouped IDMA systems is demonstrated in Figure 9. From Figure 9 it may be observed that coding improves the performance of OFDM-IDMA system by almost 1.5dB and SCFDMA-IDMA system by approx 2dB. Thus, applications requiring higher BER performance may incorporate coding technique. Next, comparison of the performance of MITA interleaver and FLRITI is carried out in coded environment for varying users and is shown in Figure 10. It can be deduced from the plot that even for coded systems performance of MITA interleaver is better than FLRITI for larger number of users.

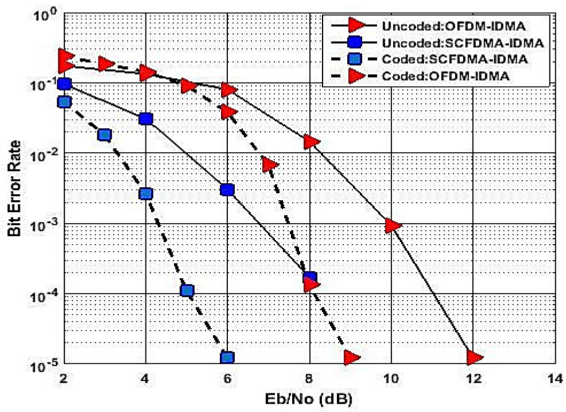


Figure 9. Comparison of BER of coded and uncoded grouped IDMA systems using MITA interleaver

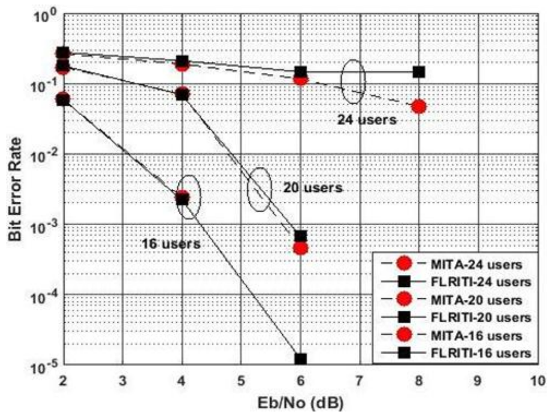


Figure 10. BER performance of MITA and FLRITI interleaver for various users over coded SCFDMA-IDMA system

4.3. Analysis of computation complexity

Computation complexity is explained as the total count of clock cycles required to generate interleaving patterns for specific number of users. The comparison of random, tree, FLRITI and MITA interleaver in tabular form is presented in Table 3. From the Table 3 it is evident that MITA has lesser computation complexity than Tree and FLRITI. This is due to the fact that more interleaving patterns can be generated with less clock cycles in MITA interleaver as it incorporates reciprocity principle and also has modified structure. Although Random interleaver has the lowest complexity but it is less preferred as the bandwidth required is proportional to user count. For the same bandwidth requirement, MITA has lower computation complexity and hence is a viable option. Computation complexity is of a major concern in IDMA system as the receiver encompasses turbo processor which iterates for multiple times to improve the systems performance. Thus, an interleaver having low computation complexity without any compromise in the BER performance is a blessing for IDMA scheme.

Table 3. Clock cycles required for interleaver generation

S. No	User count	Random interleaver	Tree interleaver	FLRITI	MITA interleaver
1	2	1	1	1	1
2	6	1	2	2	2
3	14	1	3	3	2
4	30	1	4	4	3
5	62	1	5	5	4
6	126	1	6	6	4

5. CONCLUSION

The main goal of the paper was to evaluate the performance of MITA interleaver over grouped IDMA systems using QPSK modulation and to emphasize its applicability in 5G systems. The simulation results establish that MITA interleaver has better BER performance and low complexity as compared to random, tree and FLRITI interleavers, which are the prime requirements of 5G technology. The observation from the MATLAB plots suggests that as number of users increases performance of MITA gets much better than FLRITI and the former can be preferred in IDMA systems. As an extension of the work, MITA interleaver can be implemented over 5G techniques.

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