

High efficient and high gain boost converter with soft switching capability connected to grid using dq axis current control

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ABSTRACT

Renewable sources like solar PV arrays are generally operated at low voltages due to safety issues. For applications such as grid connected systems, it requires boosting to high voltage which leads to reduction in efficiency. To solve this, a new high gain and efficient boost converter which is a combination of buffer capacitor, passive clamp recovery circuit to restore leakage energy in coupled inductor is presented. The magnetic field of the linked inductor stores the energy obtained from the supply. A passive clamp network recovers the energy that is stored in the leakage inductance, enhances the gain of voltage and improves overall system efficiency. High duty ratios are not essential to achieve higher voltage gain, hence the reverse recovery problem of diode is prevented. Moreover, passive clamp network decreases the voltage stress of switch, thus a minimum rating switch be used, as a result, the system's total efficiency improves. This converter output is fed as input to a single phase full bridge inverter and also synchronized to a single phase grid by using d-q axis current controller. The performance and powers injected are analyzed by connecting a resistive load.

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1. INTRODUCTION

Since previous two decades, electricity demand increased drastically. This eventually led to excess consumption and depletion of non-renewable fuels. These served as a strong reason for the researchers to shift to solar PV panels, wind energy, and other renewable energy sources. But they suffer with major challenges such as, Because of the nonlinear features, efficient use of the source is critical. There is a need to use MPPT in order to observe peak power of a PV module [1]. They are generally operated at low output voltages (typically 30-50 V). As a result, using them for a variety of applications such as grid-connected systems and stand-alone applications becomes challenging due to the high voltage boosting requirement [2].

In order to increase the voltage level to required level, a boost converter is required. However, there are certain drawbacks in using traditional dc-dc converters, like, on the supply side, large peak current flows, deteriorating magnetic components such as inductors and eventually leading to substantial losses. Across the switch, a high voltage appears. The switch on state resistance is proportional to square of the voltage rating. Due to high voltage, on state resistance of switch also increases which increases the conduction losses. Moreover, operation of converter at large duty cycles increases the losses in parasitic resistances of components. To increase the voltage level, it is essential to design and study new high gain, efficient boost converters. Some of the following methodologies are implemented to obtain high voltage at converter output.

They cause a large ripple in the current due to leakage inductance and also spikes in voltage across the switch during turn on and comparatively bulky and costly [1]-[3]. Use of coupled inductors. They utilize the high reluctance core due to air gap and stores the energy in magnetizing inductance of the core and uses turns ratio. But they have high leakage inductance resulting in increase of losses [4], [5]. Use of interleaved coupled inductor: They uses comparatively smaller values of inductances, reduces useful for applications requiring high power [6]. To restore the leakage energy, active clamp is used. But due to conduction losses in power switch, generally passive clamp network is preferred [7], [8]. Intermediate storage capacitors can be employed to store energy and transfer to load and results in boosting of voltage at moderate duty ratio values [9]-[13].

2. METHOD

Solar PV systems have a modest efficiency (about 14–28 percent). As a result, in order to maximize the utilization of photovoltaic generated power, an efficient power conversion system is required. The novel converter (boost) topology with maximum gain comprising a coupled inductor (L_1 , L_2), one passive clamp recovery network (C_{cl} and D_{cl}), and a buffer capacitor (C_{int}) shown in Figure 1(a), where in L_1 and L_2 are inductances (primary and secondary) of a connected inductor. Passive clamp recovery of L_1 is denoted by C_{cl} and D_{cl} . The output capacitor is C_{out} , and the output diode is D_o . V_{out} is the voltage across the load. On secondary side, the buffer capacitor C_{int} and diode D_{fb} are connected. Gain ratio (n) is given by: $n=VL_2/VL_1$. In mode-I, as in Figure 1(b), MOSFET switch is kept on, current passes by means of switch and coupled inductor primary winding (L_1), energizing coupled inductor's magnetizing inductance (L_{mag}). D_{cl} and D_o are reverse biased in this mode, while D_{fb} is forward biased. L_2 and C_{cl} charges the intermediate capacitor C_{int} through D_{fb} . D_{fb} switches off when the voltage across C_{int} equals the sum of the voltages across L_2 and C_{cl} . In mode-II, as shown in Figure 1(c), the magnetizing current flowing through the primary inductor L_1 charges the switch parasitic capacitance.

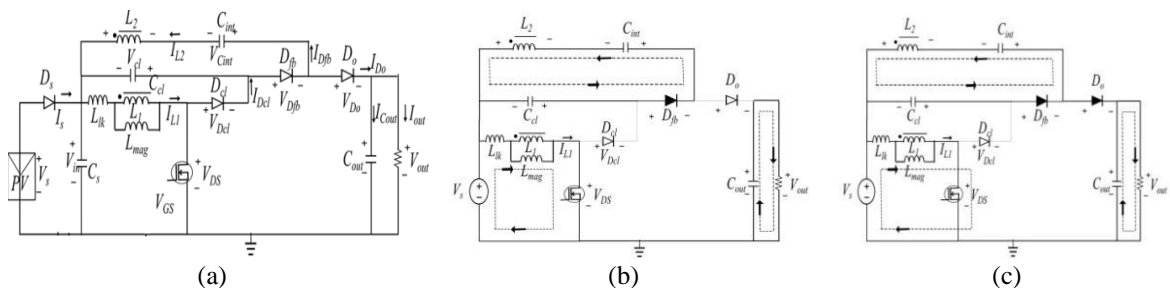


Figure 1. The novel converter (boost) topology; (a) high gain and high efficient novel converter (boost dc-dc) with coupled inductors and passive clamp circuit, (b) mode I operation of the novel converter (boost dc-dc) and (c) mode II operation of the novel converter (boost dc-dc)

The feedback diode D_{fb} remains in forward bias, current flows through supply, inductance (magnetizing) and parasitic capacitance of MOSFET switch. Diodes D_{cl} and D_o become forward biased in mode-III as shown in Figure 2(a). D_{fb} is reverse biased. The primary side coupled inductor (L_1) leakage energy is collected through D_{cl} and stored in the C_{cl} . Furthermore, as illustrated in Figure 2(b), Mode-IV begins after the leakage energy from coupled inductor L_1 has been fully recovered. While diode D_{cl} gets reverse biased, diode D_o remains forward biased. Current flows from input to the load side through inductor L_2 , intermediate capacitor C_{int} , and then to the load.

Mode-V as seen in Figure 2(c) the magnetizing current energizes the leakage inductor, while the switch parasitic capacitance discharges. Diodes, D_{cl} and D_{fb} , both are reverse biased. When the output diode D_o gets reverse biased and current direction through inductor L_2 reverses, this mode ceases shown below in Figure 2. The converter's mathematical analysis is required in order to design the components that would be employed in its construction. All of the converter's components are considered to be ideal. During switch on state:

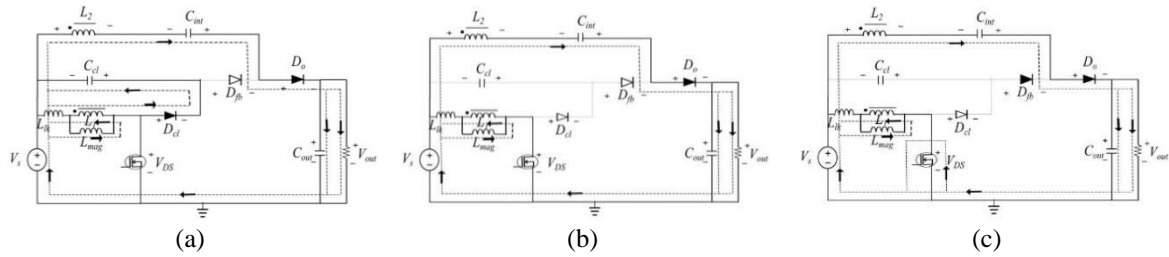


Figure 2. Operation of the novel converter (boost dc-dc); (a) mode III operation, (b) mode IV operation, (c) mode V operation

$$V_{L1} = V_S \quad (1)$$

$$V_{L2} = V_{Cint} - V_{Ccl} \quad (2)$$

As per gain ratio, $V_{L2} = nV_S$

During switch off state:

$$V_{L1(off)} = -V_{Ccl} \quad (3)$$

Applying KVL in mode 3 gives:

$$V_{L2} = V_S + V_{Cint} - V_{out} \quad (4)$$

By substituting V_{Cint} from (3), (4),

$$\begin{aligned} V_{L2} &= V_S + nV_S + V_{Ccl} - V_{out} \\ V_{L2} &= V_S + nV_S - V_{L1(off)} - V_{out} \end{aligned} \quad (5)$$

From gain ratio,

$$V_{L1} = \frac{V_{L2}}{n} \quad (6)$$

By substituting (6) into (7),

$$V_{L1(off)} = \frac{(V_S - V_{L1(off)} + nV_S - V_{out})}{n} = \frac{(V_S + nV_S - V_{out})}{(n+1)} \quad (7)$$

Voltage gain:

Across primary inductor L1, on applying voltage-second balance, we get:

$$V_{L1(on)} \cdot d + V_{L1(off)} \cdot (1 - d) = 0$$

Substituting (2) and (8) in above equation, we get

$$\begin{aligned} V_S \cdot d + \frac{(V_S + nV_S - V_{out})}{(n+1)} (1 - d) &= 0 \\ \frac{V_{out}}{V_S} &= \frac{n+1}{1-d} \end{aligned} \quad (8)$$

Where; d is duty ratio, n is gain ratio

A turns ratio is chosen for an input and output voltage requirement, and the duty ratio be computed using in (9). The magnetizing inductance value

$$L_{mag} = \frac{1}{2} * \frac{V_s * d}{\Delta I_{mag} * f_s} \quad (9)$$

The minimum value of the clamp capacitor

$$C_{cl} = \frac{I_{mag} * d_{lk}}{\Delta V_{ccl} * f_s} \quad (10)$$

The minimum value of the energy storage capacitor

$$C_{int} = \frac{I_{mag} * d}{n * \Delta V_{cint} * f_s} \quad (11)$$

The minimum value of the output capacitor

$$C_{out} = \frac{I_{out} * d}{\Delta V_o * f_s} \quad (12)$$

The minimum required value of output capacitance

$$C_{out(min)} = \frac{\Delta I_o * x T_s}{0.01 V_o} \quad (13)$$

Where T_s hold-up time corresponding to load transient of ΔI_o .

For $V_s=35V$, $V_{out}=350V$, $n=4$:

In (8), $\frac{V_{out}}{V_s} = \frac{(n+1)}{(1-d)}$, We get $d=0.5$

In (9), $L_{mag} > \frac{1}{2} * \frac{V_s * d}{\Delta I_{mag} * f_s}$, We get, $L_{mag} > 48\mu H$

In (10), $C_{cl} = \frac{I_{mag} * d_{lk}}{\Delta V_{ccl} * f_s}$ we get $C_{cl}=1\mu F$

In (11), $C_{int} = \frac{I_{mag} * d}{n * \Delta V_{cint} * f_s}$ we get $C_{int}=47\mu F$

In (12), $C_{out} = \frac{I_{out} * d}{\Delta V_{out} * f_s}$ we get $C_{out}=180\mu F$

With converter parameters as per Table 1, voltages across and current through capacitors, diodes and inductance are obtained as: Reverse voltage across switch S is $V_{DS} = \frac{V_s}{(1-d)} = 70$ V, Reverse voltage across D_{cl} is $V_{dcl} = \frac{V_s}{(1-d)} = 70$ V, Peak current through D_{cl} is $I_{dcl} = \frac{V_{ccl} * d_{lk}}{L_1 * f_s} = 5.6$ A, Peak current through L_{mag} is $I_{Lmag} = \frac{V_s}{L_{mag}} * d T_s = 7$ A, Peak current through L_1 is $I_{L1} = \frac{n}{2} * I_{Lmag} = 14$ A, Reverse voltage across D_{fb} is $V_{dfb} = 2nV_s = 280$ V, Peak current through D_{fb} is $I_{dfb} = \frac{(V_{cint} - V_{ccl}) * d}{n * L_2 * f_s} = 2.25$ A, Reverse voltage across D_o is $V_{do} = \frac{n}{(1-d)} V_s = 280$ V, Peak current through D_o is $I_{do} = \frac{(V_{out} - V_{ccl} - V_s) * (1-d-d_{lk})}{n * L_2 * f_s} = 1.5$ A, Voltage across C_{cl} is $V_{ccl} = \frac{d}{1-d} V_s = 35$ V, Voltage across C_{int} is $V_{cint} = \frac{d(1-n)+n}{(1-d)} V_s = 175$ V.

Table 1. Converter specifications

Parameter	Value
Source dc voltage	35 V
Output voltage	350 V
Coupled inductor turns ratio	4
Switching frequency	50 kHz
Coupled inductor	Magnetizing inductance $L_{mag} 50 \mu H$
Clamp capacitor	1 μF
Intermediate capacitor	47 μF
Output capacitor	180 μF

The operation of the novel converter is compared with boost converter in terms of parameters given as per Table 2. But in practical application circuits, the inductor in conventional boost converter will not be

perfectly inductive with zero internal resistance due to which the maximum operating duty ratio of the traditional boost converter will be restricted to (0.4-0.6). As a result, we can't operate at 0.9 duty cycle practically, and thus can't obtain large voltage gain using the traditional converter. The switch drop and switching losses obtained are high. So it causes high loss switching. Hence it is clear that the novel topology is superior in performance.

Table 2. Values of simulation

Parameters	Values
Switching frequency	5 kHz
Couple inductor turns ratio	4
Filter inductance	1 mH
Filter capacitor	5 μ F
AC peak voltage	324 V
Resistive load active power	500 W
Resistive load reactive power	0 VAR
Module peak power	240 W
Open circuit module voltage (V_{oc})	51V
Short circuit module current (I_{sc})	6.3 A
MPP voltage of module (V_{mp})	42.8 V
MPP current of module (i_{mp})	5.6 A
Peak power of array (P_{mp})	1200 W
Open circuit array voltage (V_{oc})	51 V
Short-circuit array current (I_{sc})	31.5 A
MPP voltage of array (V_{mp})	42.8 V
MPP current of array (I_{mp})	28.03 A

3. GRID SYNCHRONIZATION

The following Figure 3 depict the complete block diagram of the system with synchronization and resistive load. The grid current is sensed and converted into two orthogonal signals I_α, I_β [14]-[25] by introducing a transport delay of 90° . $I_\alpha = A \sin(\omega t + \phi)$ $I_\beta = A \sin(\omega t + \phi - \frac{\pi}{2})$. The signals are transformed to dq reference frame to get corresponding current signals by using parks transformation
$$I_{dq} = \begin{bmatrix} I_d \\ I_q \end{bmatrix} = T I_{\alpha\beta} = \begin{bmatrix} \sin \omega t & -\cos \omega t \\ \cos \omega t & \sin \omega t \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix}.$$

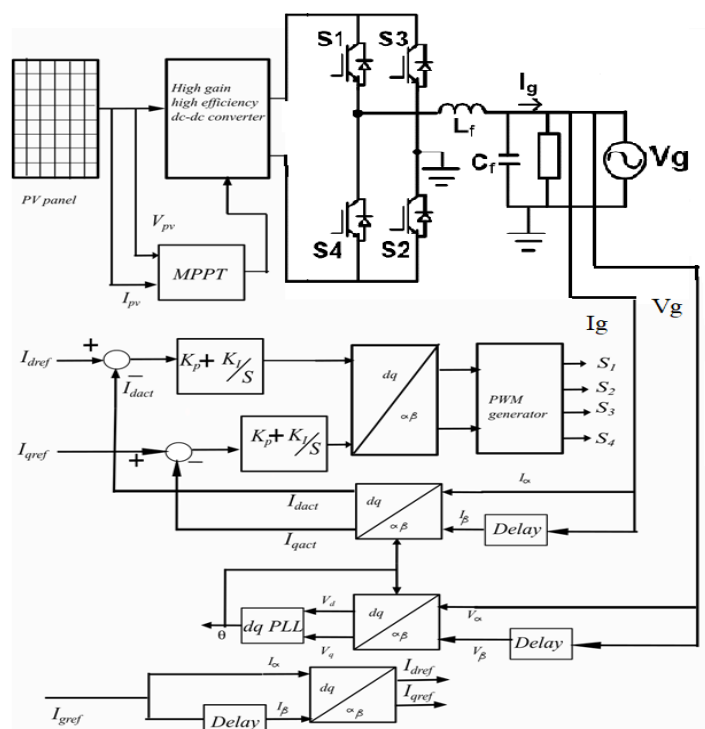


Figure 3. Proposed control scheme for management of power flow of a grid connected PV system

The grid voltage V_g is given as input to phase locked loop to get corresponding phase angle. The actual current signals are compared with current signals obtained from the grid reference current [14]-[18]. The obtained errors are minimized using proportional-integral controllers. The output signals are transformed to stationary frame using inverse parks transform shown below. The below output generates the required reference wave to the PWM generator and compared with carrier wave and generates the switching pulses and thus controls the output voltage of the full bridge inverter.

$$I_{\alpha\beta} = \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = T^{-1} I_{dq} = \begin{bmatrix} \sin \omega t & \cos \omega t \\ \cos \omega t & -\sin \omega t \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix}$$

4. RESULTS AND DISCUSSION

The converter is analyzed in simulation with MATLAB/Simulink environment. Figure 4 shows the complete simulation model of the system with detailed described parameters in Table 3. The waveforms of current and voltage supplied by the PV array is shown in Figure 5. Outputs of switch voltage, magnetizing current, voltage through diode and voltages of clamped capacitors during various operational modes are shown in Figure 6, Figure 7 and Figure 8. Efficiency at full load is obtained as 94% shown in Figure 9.

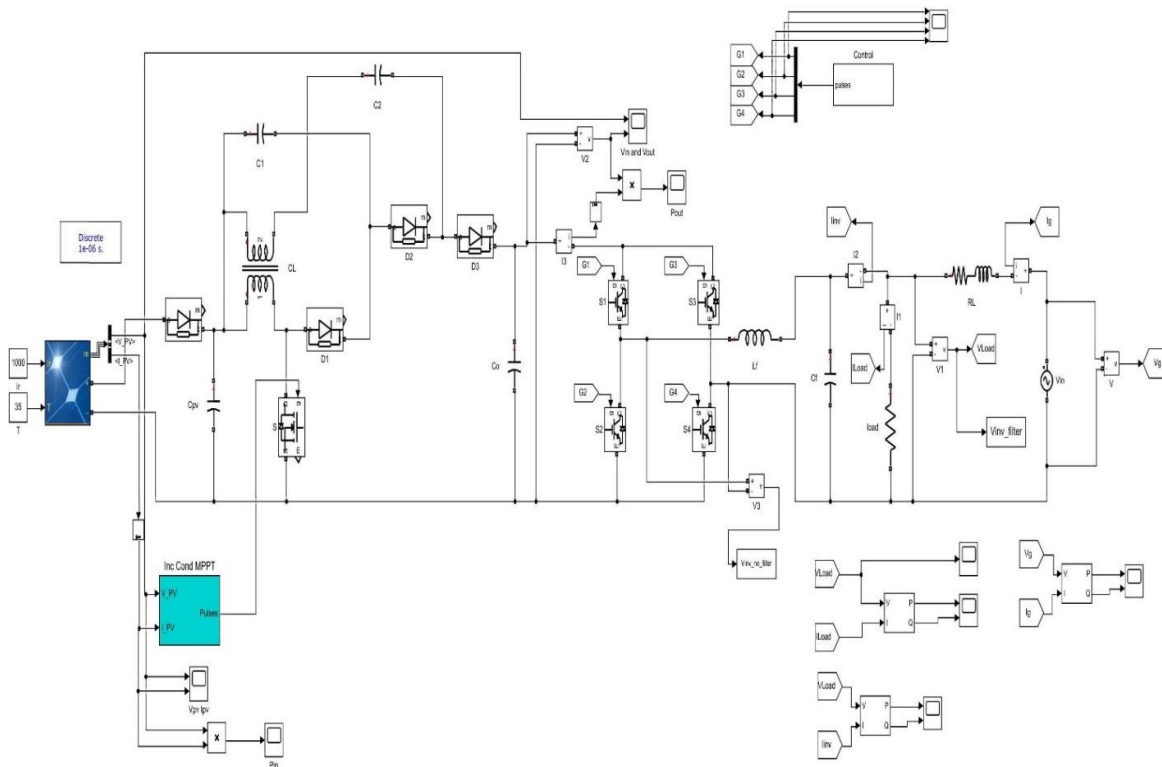


Figure 4. Simulation model of the overall system

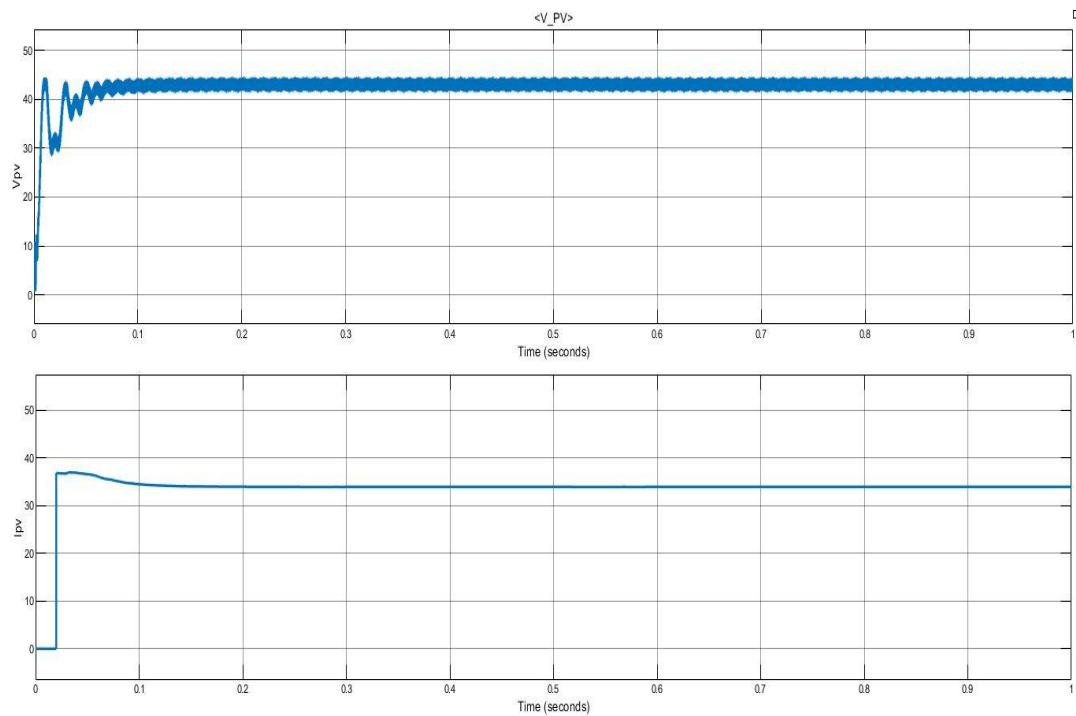


Figure 5. Input voltage and current waveforms

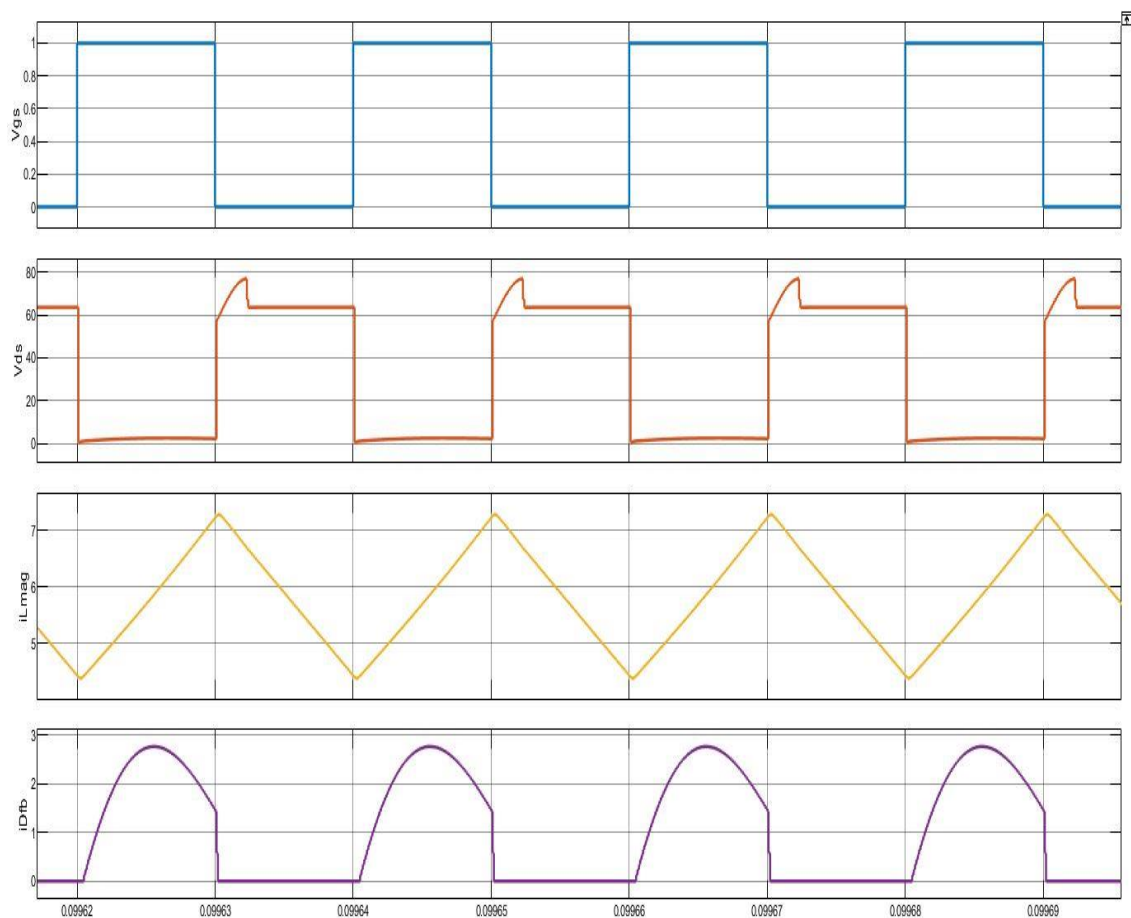


Figure 6. Waveforms of; (a) gate to switch voltage, (b) switch voltage, (c) magnetizing current, (d) current through feedback diode

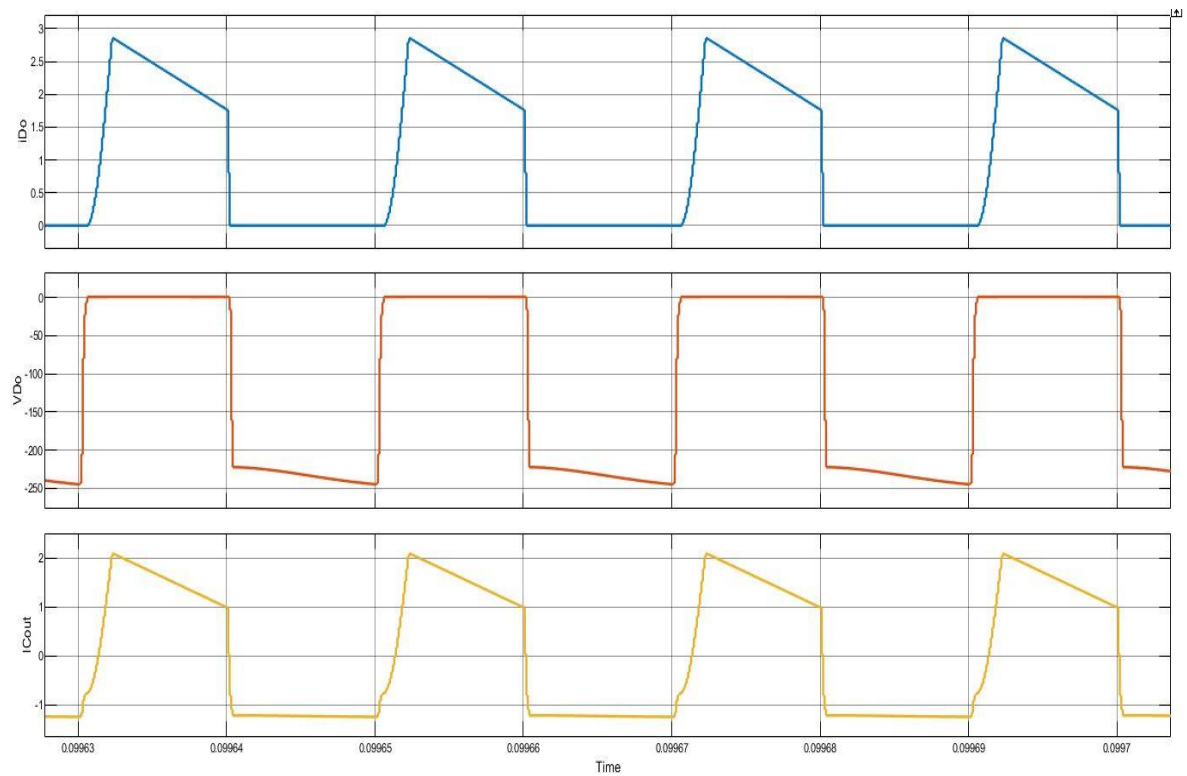


Figure 7. Waveforms of; (a) current through output diode, (b) voltage across output diode, (c) current through output capacitor

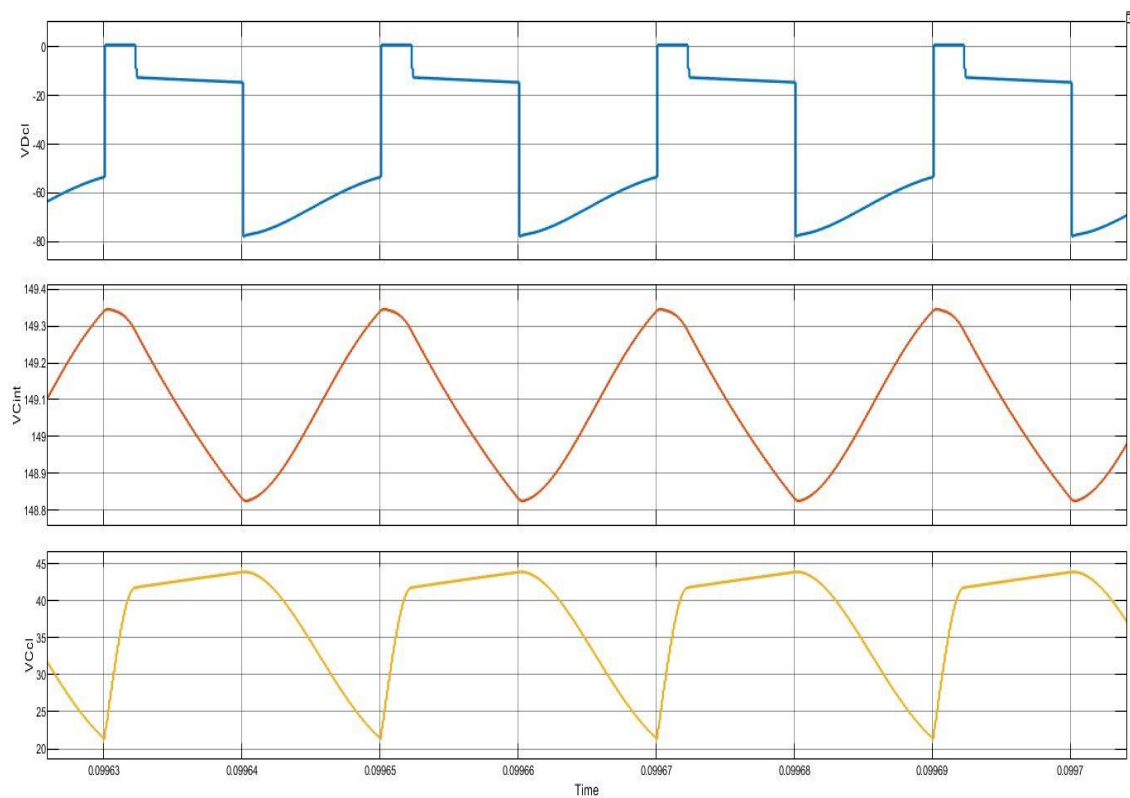


Figure 8. Waveforms of; (a) voltage of clamp diode, (b) voltage of intermediate capacitor, (c) voltage of clamp capacitor

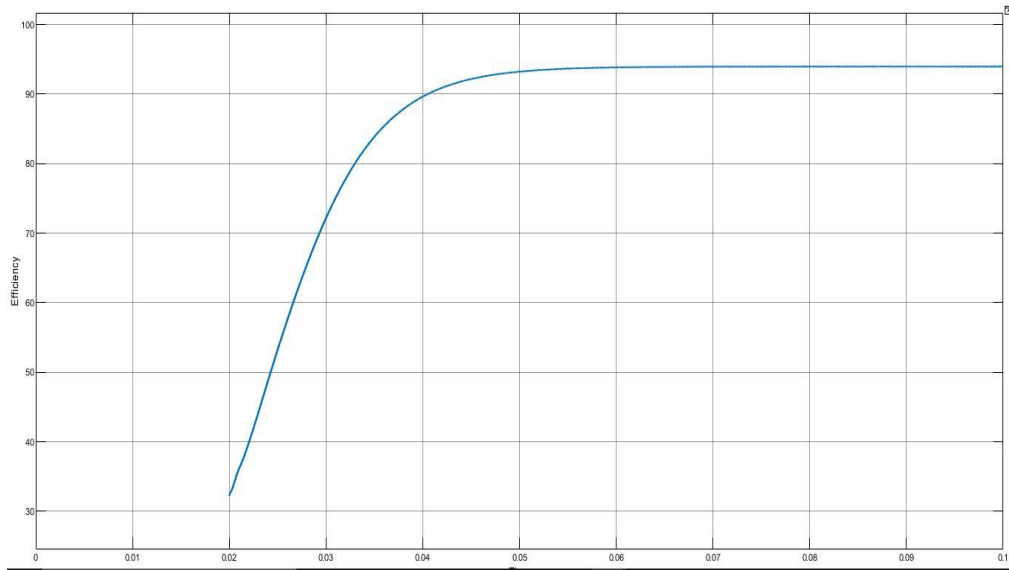


Figure 9. Efficiency of high gain dc-dc converter

Design of LC filter: Filter inductance is designed based on limiting ripple in load current to 20 % of the rated current.

$$L = \frac{V_{dc}}{4f_{sw}\Delta I_{ppmax}} = 1 \text{ mH}$$

Under rated condition, the reactive power that can be absorbed must be restricted to 5% of rated power, therefore filter capacitance is calculated accordingly.

$$Q = \frac{V^2}{X_c} = V^2 \cdot 2\pi f C$$

$$C = 5 \mu\text{F}$$

Table 3. THD before and after LC filter

	THD
Before filter	52.08%
After filter	4.62%

By employing the filter, square wave output wave of inverter is converted to nearly sinusoidal signal and higher order harmonics are eliminated. THD obtained is 4.62%, FFT analysis is presented below in Figure 10 and Figure 11.

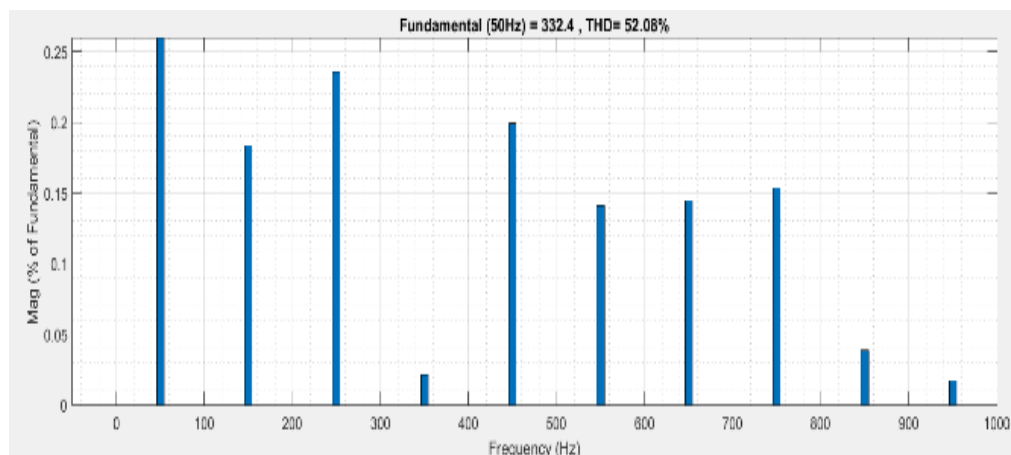


Figure 10. THD of voltage waveform without LC filter

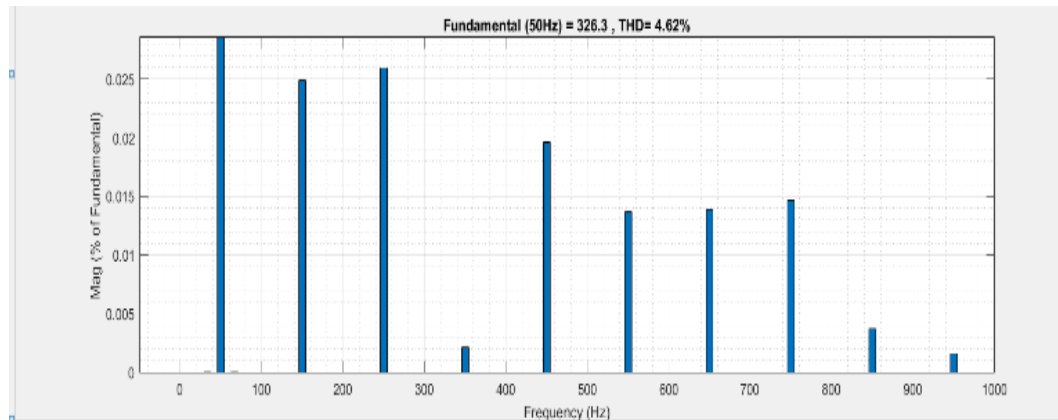


Figure 11. THD of voltage waveform with LC filter

The system is tested during both light load and overload conditions. During light load conditions, the excess power output from the inverter is fed to grid and hence the grid power appears as negative in the waveform. During overload conditions, the inverter supplies a portion of the load's required power, while the grid supplies the remaining active power, as indicated below in Figure 12 and Figure 13.

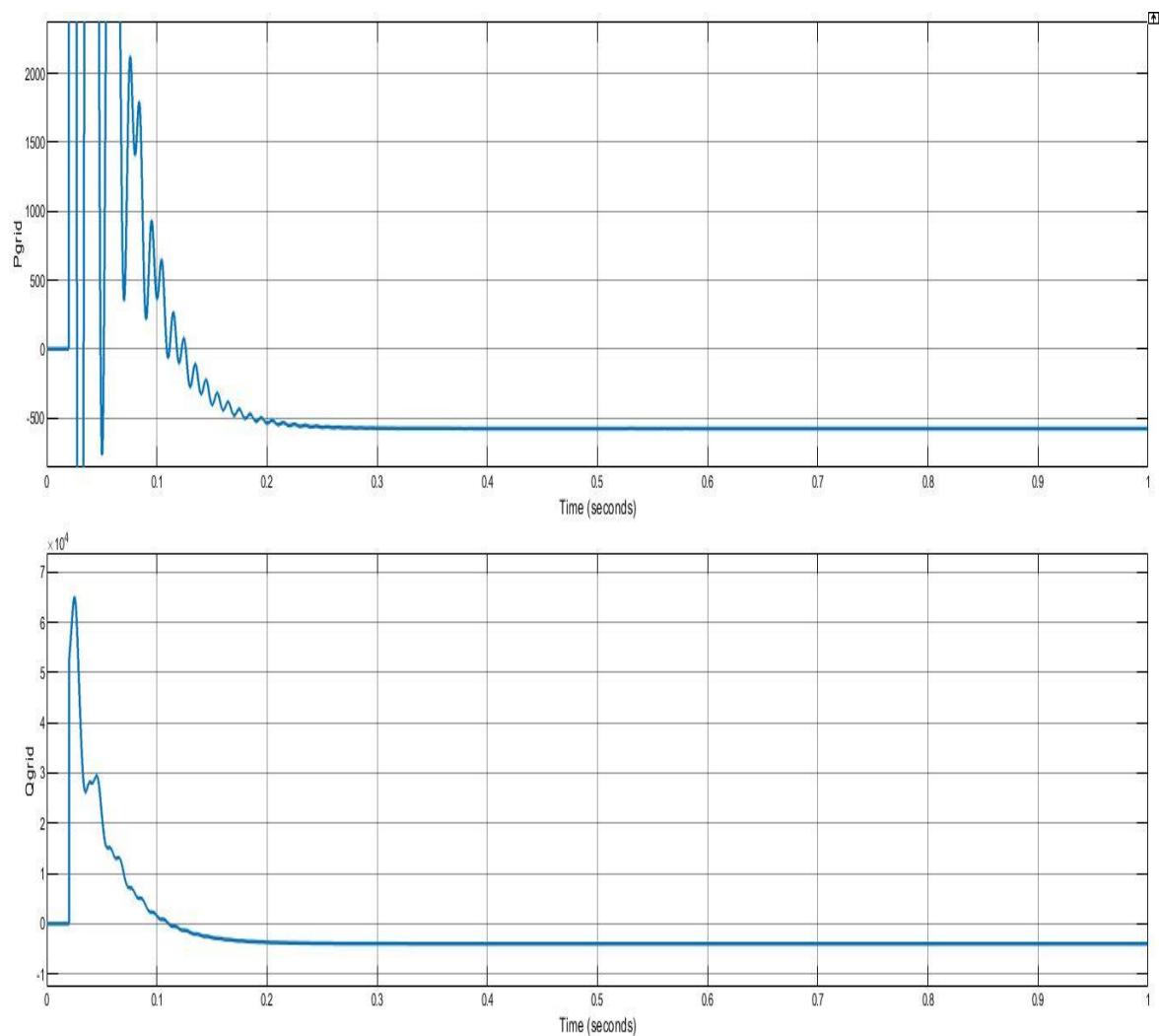


Figure 12. Power injected to grid (light load conditions)

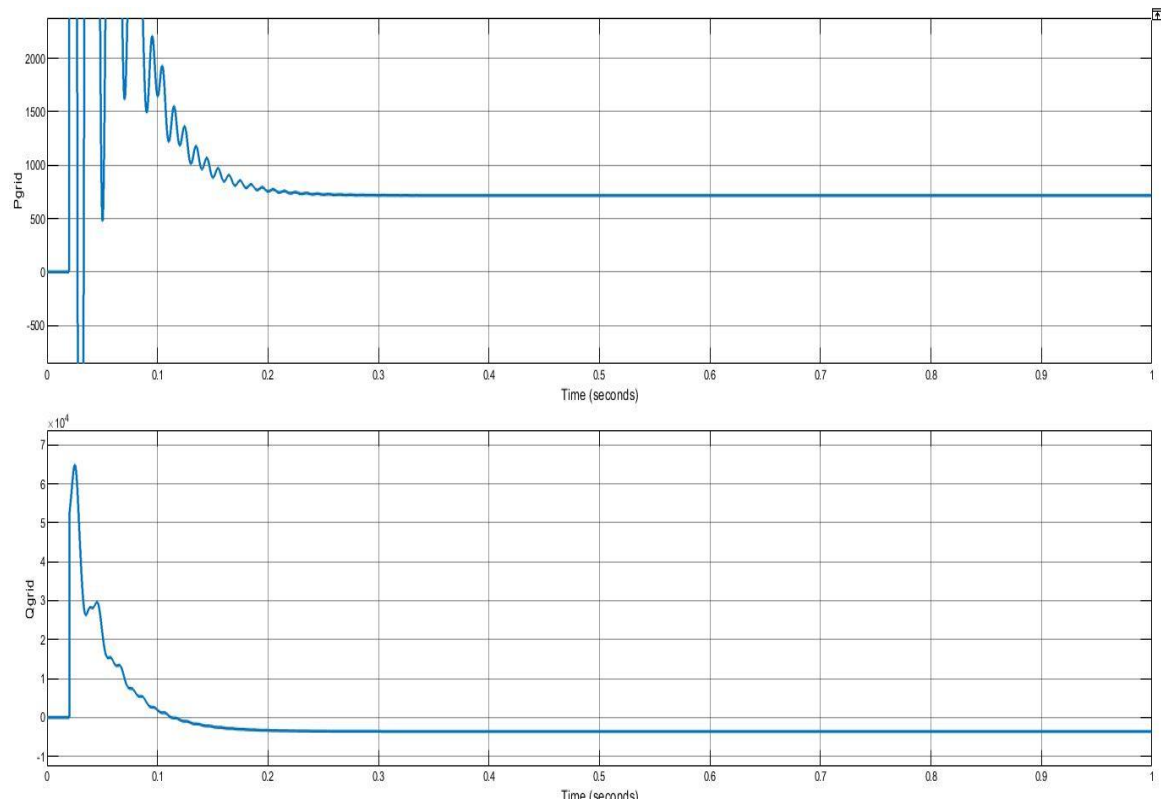


Figure 13. Power injected by grid to load (over load conditions)

5. CONCLUSION

Novel converter with large gain implemented for low and medium-voltage source applications. High gain is obtained at lower duty cycles with minimum switching is obtained. The efficiency of dc-dc converter at full load is obtained as 94%. Output voltage, diode currents and voltages, capacitor voltages are calculated. The converter is fed to a single phase full bridge inverter, which is then connected to the grid. The system is synchronized to grid by using d-q axis current control. The switching pulses to inverter are obtained from pulse generator based on d-q axis control. Waveforms of output voltages and power of R load with and without LC filter are observed at light load and overload conditions and THD is seen. PV-source with incremental conductance method is used as input to novel high gain boost converter using d-q axis controller and all required characteristics are observed. The proposed converter's performance is verified in a simulation environment, and the findings are presented.




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