

Delta-sigma ADC modulator for multibit data converters using passive adder entrenched second order noise shaping

Ali Kareem Nahar, Hussain K. Khleef

Department of Electrical Engineering, University of Technology, Baghdad, Iraq

Article Info

Article history:

Received Mar 1, 2021

Revised May 20, 2021

Accepted Jun 18, 2021

Keywords:

2nd Order noise shaping

DWA

MDC

$\Delta\Sigma$ -DAC modulator

ABSTRACT

This paper introduces a multi-bit data converters (MDC) modulator of the 2nd order delta-sigma analog-to-digital converter use the passive adder proposed. The noise shaping quantizer can provide feedback that has generated quantization noise and perform additional shaping noise first-order by coupling noise method. Thus, two Integrator's with ring amplifier and the MDC is shaped by noise coupling quantizer know the 2nd-order noise coupled with somewhat of a DAC modulator. At a summing point, the inputs are summed and then filtered with a low pass filter. A cyclic second order response is generated with a data weighted averaging (DWA) technique in which the DACs' outputs are limited to one of two states in the noise shaping responses. Mainly as a result of the harmonic distortion in circuits of amplifier. Transistor rate is equipped for the fully differential switched condenser integrator used, a comparator and DWA. The modulator with proposed DWA design, almost quarterly improved timing margin. A simulated SNDR of 92dB is obtained at 20 MHz sampling frequency; while a sinusoidal output of 4.112 dBFS is tested at 90 μ s besides 20 MHz as the bandwidth. The power consumption is 0.33 mW while the voltage of the supply is 1.2V.

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Corresponding Author:

Ali Kareem Nahar

Department of Electrical Engineering

University of Technology

Baghdad, Iraq

Email: alikareemnahar79@gmail.com

1. INTRODUCTION

Wideband high-resolution analog-to-digital converter (ADC) are normally used in both the wireless communication network and image sensor fields in the mixed-signal SoC [1]. The ADC is extensively used in mixed-signal circuits as an interface between the digital and analog domains [2]. However, the decrease in supply voltage in deep-submicron CMOS technology naturally degrades ADC's accuracy. $\Delta\Sigma$ -DAC modulators appreciate high resolution by noise shaping technique and oversampling. In the deep submicron CMOS systems, which are the most suitable for high resolution applications [3]. Since MDC ADC resolution depends on condenser matching accuracy and comparator offset, in nano-scale CMOS technology, achieving a high-resolution ADC is difficult. Of fact, since the $\Delta\Sigma$ -ADC modulator uses an oversampling and noise shaping technique to minimize quantization noise in the target signal band, it is ideal for high SNDR ADC in nanometre CMOS technology [4].

The feedback network's resistance was deliberately selected to avoid signal distortion at the output voltage. The low pass filter was added after the differential amplifier to reduce noise from the ADC driver. This demonstrates that the AD8139 can be used as an ADC driver for a differential 10-bit SAR ADC [5], [6]. On the other side, the high SNDR modulator is generated using high-order noise-shaping techniques and a

lower over-sampling ratio (OSR). High OSR, on the other hand, necessitates high-speed operation, which increases the modulator's overall power consumption. Many methods have been suggested to boost the SNDR and reduce the $\Delta\Sigma$ -DAC modulator's power consumption [7]. The integrator's output swing is minimized using feed forward architecture, which can ease the amplifier's linearity specifications in the integrator, thereby decreasing the $\Delta\Sigma$ -DAC modulator's power consumption. Similarly, error feedback system, noise coupling was suggested to actively form the noise characteristic of the $\Delta\Sigma$ -ADC modulator [8]. The noise coupling technique performed by SAR ADC has been proposed in recent researches [9] for MDC-DAC has the desirable characteristics when a successive approximation is complete, this may hold the quantization noise. The works previously reported [10], [11] include remainder, the active buffer circuit and sampling complement the large amount of energy consumed. Despite the fact that digital domain noise coupling techniques will eradicate the drawbacks of analog domain noise coupling techniques, a terminated 5-bit DAC SAR is used as a 4-bit internal quantizer for quantizing noise [12]. The voltage changes in the modulator are significantly reduced by adding direct forward feed of the input signal to a quantizer. It is therefore possible to overcome the drawbacks of $\Delta\Sigma$ -DAC modulators [13].

An approach is proposed in this work, to carry out the multibit data converters (MDC) quantization noise coupling. The noise coupling process suggested is carried out in the analog domain, and then it eliminates the limitations of the preceding methods of analog domain noise coupling. Furthermore, the use of the dynamic amplifier to realize the maximum power output of the amplifier in DAC [14], [15]. The temperature sensing center, amplifier, and ADC are all part of the thermal detector design. The sensor was created using 0.13 m CMOS technology and works by sensing the processor's temperature and producing a digital output value [16], [17]. To suppress spurs without in-band noise, a modulator with low pass dither shaper is introduced. In addition, 2nd-order noise is mixed passive adder entrenched modulator $\Delta\Sigma$ -DAC with dual integrator-based analog dynamic mechanisms and a quantizer embedded passive adder. Two ring amplifier integrators are used to achieve 2nd-order noise shaping in a behavior-level modeling process. The modelling of each block in $\Sigma\Delta$ -CAD facilitates the easy design with 20 MHz bandwidth and the estimation of the non-ideal effects, which may arise in the design of the circuit and the following procedures. Using the proposed MATLAB model, the effect of the proposed modulator on the $\Sigma\Delta$ -DAC can be readily identified quantitatively.

2. PROPOSED $\Delta\Sigma$ -ADC MODULATOR ARCHITECTURE

The sigma-delta oversampled ADC is a noise-shaped quantizer. The main goal of noise shaping is to reshape the quantization noise spectrum and filter out the majority of the noise from the right frequency range, such as the speech applications audio band. The main objective is to increase sampling rate thereby lowering the amount of bits per sample. A sound-shaping quantizer compensates for the resulting increase in quantization noise. The added quantization noise is moved out of the corresponding frequency band by this quantizer, which preserves the desired signal quality level [18]. The decrease in bits simplifies the AD and DA converter design. As seen in this example, an initializing profiteer prefers an analog input structure is basic by over-sampling. The output signal is suppressed by a 64 factors. Zero-order hold blocks, integrator, and 4-bit quantizer consist of a DAC of two stages. The analog input subtracts the value of the zero-order hold. The feedback or approximation loop causes high-pass filtering of the quantization noise produced by the ADC, moving the energy from the corresponding signal band to the higher frequencies. The platform of decimation reduces the rate of sampling to 2 MHz. This eliminates the high-frequency quantization noise produced during this process through any unnecessary frequency components beyond $f_s/2$ equal (4 MHz) that the simple analog pre-filter did not delete are removed by the feedback loop.

Figure 1 shows the proposed 2nd-order $\Delta\Sigma$ -DAC modulator block diagram. It consists of two integrators, a passive adder 4-bit MDC quantizer 2 of the DACs and logic of data weighted averaging (DWA) for simplicity. Dual integrators are used to shape the noise of the second order. The MDC quantizer integrated 4-bit passive adder is used for summation analog signal. The proposed MDC quantizer is used not only as an internal quantizer. However, it can also be used as a noise coupling circuit. The QNS circuit performs $(z-1)$ for noise quantization transfer function. The signal $(X1/2)$ is passed to the 2nd Integrator input node so that the noise is injected again into the modulator for noise shaping as 1st-order application. So, the noise tied with the $\Delta\Sigma$ -DAC modulator performs the task of noise shaping in the second order by using two integrators. The specification of a general DWA algorithm that realizes the DAC converter mismatch shaping transfer function of the form $(z-1) D$ is presented in this brief [19]. As a result, the 4-bit capacitive DAC2 for the 2nd integrator in Figure 1 is modeled without DWA as a binary-weighted-element.

applied by the three filters, according to the decimation method, is 16 (first filter)+4*16 (second filter)+16*16 (third filter), for a total latency of 336. The 'Time Delay' parameter denominator is the model's base rate (512 kHz). A four-section CIC decimator is used by the fixed-point method reducing the sampling frequency by the same 64 factors. Although not as robust as an FIR decimator, the advantage of the decimator CIC is that it does not require multiplying operations. Only additions, subtractions, and delays are used to execute it. Therefore, a hardware implementation where machine resources are limited is a better choice. The CIC decimator provides a 156 sample latency, which is the filter unit delay (154.5) that is rounded to the adjacent integer. The value is used in the block 'Multistage CIC Processing Delay' parameter 'Time Delay'.

Figure 3 displays the schematic diagram of the MDC quantizer integrated with the proposed passive adder. It consists of QNS chain, dynamic comparator, capacitive DAC, and SAR logic asynchronous circuits. Figure 3 (a) demonstrates a condenser array's analogous circuit there are two modes of operation for the passive adder, when the MDC circuit is made up of three parts of capacitors. Figure 3 (b) displays the block diagram for the MDC circuit of the clock generator. Figure 3 (c) demonstrates the MDC circuit's corresponding circuits in four operation states types S_0 , S_1 , S_2 and S_3 sets.

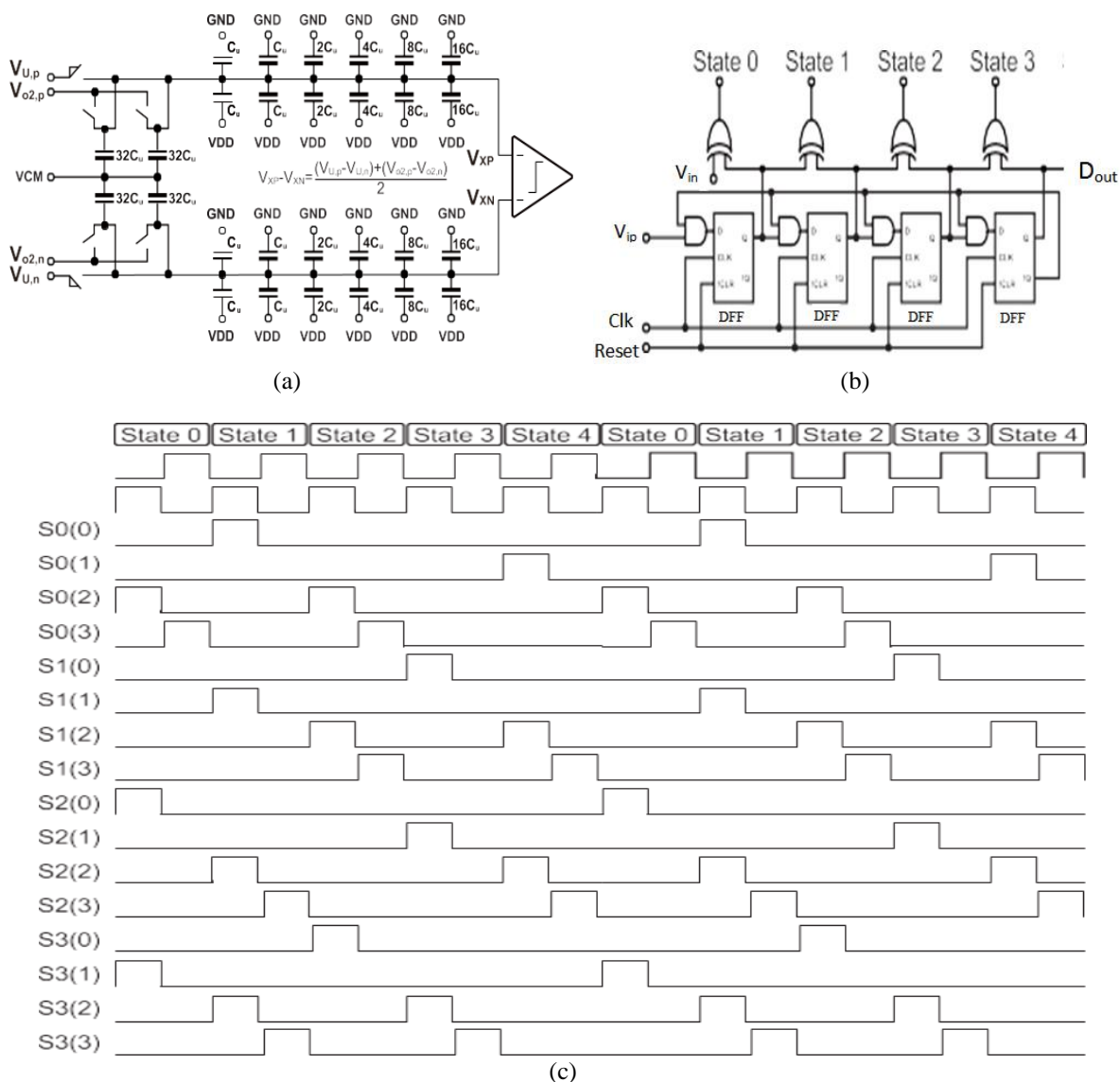


Figure 3. Operation of the circuit recommended by the MDC; (a) sampling mode SAR DAC equivalent circuit, (b) MDC circuit clock generator, and (c) MDV circuit clock schedule

4. SIMULATION RESULTS

CMOS equipment was designed for the proposed 2nd-order upper DAC modulator. Taking into account the factors listed in Table 1 based on MDC quantizer, Figure 4 displays the power output spectral density of two $\Delta\Sigma$ -DACs. Transistor-level spice simulations were performed to validate the modulator's performance and to check the proposed architecture's effectiveness. To achieve high resolution and target, noise shaping reduces power. The modulator has a 2nd-order loop with 4-bit DACs, 20 MHz sampling frequency, and an OSR of 18, resulting in an SNDR of 92.6 dB in the perfect case. Figure 5 shows a correlation of MDC-DAC and ideal DAC module rate with saturation voltages=+1V. The two cases show a SNDR disparity of less than 0.4 dB, and harmonic tones of less than 10 dB. More importantly, it is clear that threshold voltage mismatches greatly affect the modulator output, with broad distortion sounds, the SNDR falls by 6 dB compared to the perfect case.

Table 1. Factors of the proposed $\Sigma\Delta$ -DAC modulators based MDC quantizer

Factor	Value
Irritating sample	0.07%
Element mismatch	1.32%
Switch noise (KT/C)	54mVrms
OTA noise	20 rms mV
Finite Dc gain	60 dB
Finite GBW	20 MHz
Finite slew rate	10 V / m s
Saturation voltages	+/- 1V

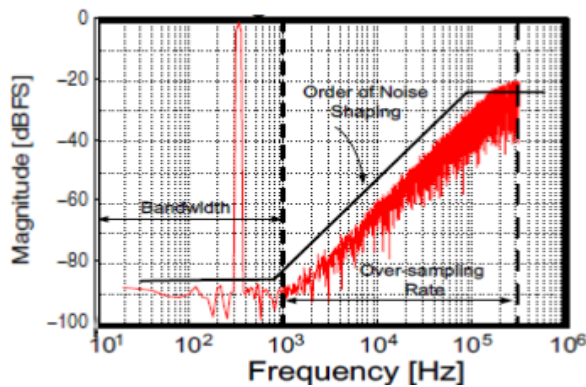


Figure 4. The power spectral density of the two $\Sigma\Delta$ -DAC

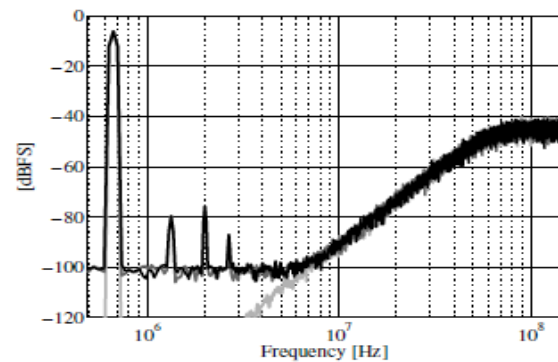


Figure 5. Simulation of the output power spectrum in Figure 1 with harmonic distortions based on the proposed second-order MDC $\Delta\Sigma$ -DAC modulator

The proposed DAC modulator works for a 200 MHz BW at a clock frequency of 2 MHz and consumes 0.33mW for both the analog circuit component and the electronic circuit portion under a supply voltage of 1.2V. Figure 6 shows the simulated spectrum effects in a 5.12dBFS and the proposed modulator SNDR. Figure 6 (a) displays the effect of the its without flicker vibration or noise. The simulation is run to represent the ambient-DAC modulator's measured performance as closely as possible, taking into account both flicker noise plus thermal noise determined by the spice simulator in accordance with the CMOS system library typical. The simulator's peak noise frequency parameter is set at 200 MHz clock speed; it controls the amount of energy that can be produced by each noise source. The simulator's minimum noise frequency parameter is set to 10 KHz, setting the lower frequency limit to the simulation of flicker noise [23], [24].

Figure 6 (b) displays the effect of the simulated spectrum with flicker noise and thermal noise. The maximum signal to noise and distortion ratio (SNDR) of 69.8 dB will be reached unless the DWA is applied. The SNDR were strengthened near 92.6 dB when a DWA is applied. Furthermore, compared to previous research in Table 2 summarizes the performance of the proposed MDC-DAC modulator. FOMW and FOMS are assessed as 22fJ/conversion and 171.2 dB respectively.

The simulations show a better FOM compared to the other related BW work. Although thermal and flicker noise, as well as capacitance mismatch, it is not a chip calculation, but it is taken into account in the simulation results of the proposed MDC-based DAC modulator. The model modulators FOM and SNDR

should be contaminated by the spice simulation performance. Signal frequency and bandwidth procedures, however, frequently exceed the comparable quality of the results of the spice simulation.

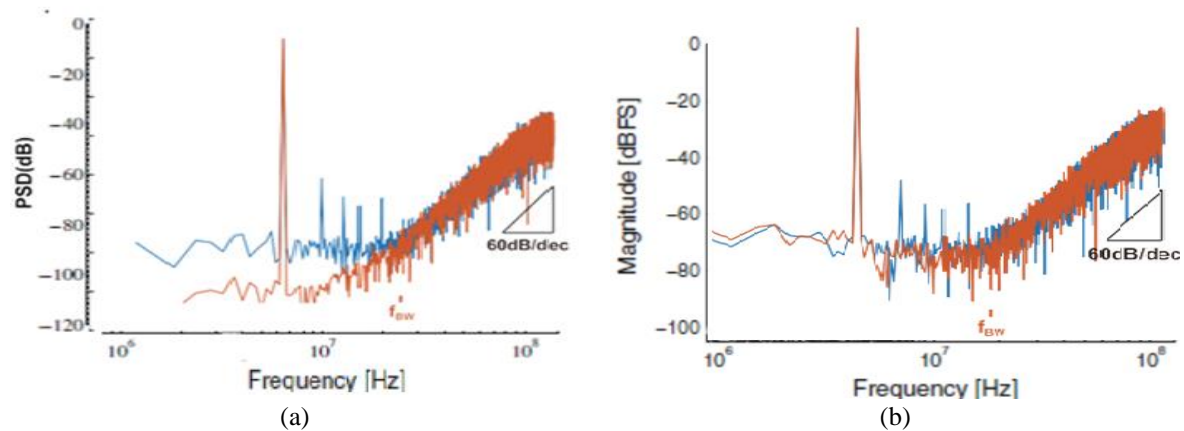


Figure 6. Simulated performance range with DAC mismatches in unit efficiency; (a) without flicker noise or thermal noise, (b) flicker and thermal noise

Table 2. Description of quality and analysis of previous works

Specification	Chen [21]	Pan and San [20]	Z. Chen, M. Miyahara and A. Matsuzawa [25]	C. Pan, and H. San [3]	A. Nahar [This work]
Process (nm)	180	90	65	90	110
Supply Voltage (V)	1.3	1.1	1	1.2	1.2
NS order	3	3	3	3	3
Sampling rate (MS/s)	25	100	50	100	100
Signal BW (KHz)	100	109	100	3125	2000
SNDR (dB)	84	77.93	74.9	91.64	92.60
Power (mW)	0.14	0.42	0.0458	0.0834	0.33
F_0M^W (fJ/conv.-step)	54	162.1	50	23.4	22
F_0M^S (dB)	172.5	169.2	168.3	179.9	19

5. CONCLUSION

This paper suggests a 2nd-order noise coupling method by using an embedded passive adder quantization noise shaping MDC, $\Delta\Sigma$ -DAC modulator with 2 dynamic-analog component-based integrators and an embedded MDC quantizer with passive adder. For the 2nd-order noise shaping, two integrators consisting of ring amplifiers are used. The proposed MDC quantizer embedded passive adder is used for summarization of analog signals, quantization, and noise quantization. Benefiting from the suggested MDC quantizer's quantization noise feedback feature, the noise coupling technique could apprehend an added 1st-order noise shaping. Using the active analog portion is not needed the proposed noise coupling technique; lower consumption can be continued. Moreover, the proposed modulator, sample clock generator only needs two non-overlapped clocks. The power consumption of the -DAC modulator circuit can be held low because it is implemented using a dynamic analog component. The test results, which included thermal and flicker noise, indicate that the proposed $\Delta\Sigma$ -DAC modulator is viable. The maximum SNDR of 92.60dB is achieved while OSR=18 is achieved with an amplitude of 4.112 dBFS for sinusoid input at 2000 kHz.

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BIOGRAPHIES OF AUTHORS

Ali K. Nahar was born in Baghdad, Iraq in June of 1979. He received his B.Sc and M.Sc degrees in 2001 and 2008 respectively In University of Baghdad and University of Technology, Iraq. From 2013-2016, he joined a PhD study at the Faculty of Electric Engineering, (UMP), Pahang, Malaysia. Since 2002, he has been a Lecturer of Electronic and communications Engineering at the University Of Technology (UOT), Baghdad, Iraq. Starting scientific publishing since 2007, he has more than 25 publications in national and international conferences and journals.



Hussain Kareem Khleaf was born in Baghdad, Iraq on March 14 of 1975. He received his B.Sc degree in 2000/2001, M.Sc degree in 2003, from University of Technology, Baghdad, Iraq, and PhD degree in 2015 from University Malaysia Bahang (UMP). Bahang, Malaysia. Professionally he has worked in several national and international companies before moving to the academia in 2006.