Bulletin of Electrical Engineering and Informatics
Vol. 10, No. 6, December 2021, pp. 2964~2971
ISSN: 2302-9285, DOI: 10.11591/eei.v10i6.2788

A single-phase simplified DC-AC converter using DC-link capacitors and an H-bridge

Sai Divya Sindhura Nunna[1], Akhilesh Ketha[2], Srivastav Sai Goud Padamat[3], K. Rambabu[4], Ujwala Anil Kshirsagar[5], Abhilash Tirupathi[6]
[1,2,3,4]Department of Electrical and Electronics Engineering, Aditya Engineering College, India
[5]Department of E&TC, Symbiosis Institute of Technology, Symbiosis International (Deemed University), (SIU), Pune, Maharashtra, India
[6]Department of Electrical Engineering, Accendere Knowledge Management Services, CL Educate Ltd., India

Article Info

Article history:

Received Jan 9, 2021
Revised May 20, 2021
Accepted Oct 20, 2021

Keywords:

DC-AC converter
Hybrid structure
Multilevel inverter

ABSTRACT

This paper introduces a simplified inverter circuit using a single dc source and an H-bridge with a least possible number of "switching devices". This topology does not employ multiple "dc sources", which enhances the reliability of the configuration. The topology consists of two parts, namely: "Level generation parts" as well as "Polarity generation parts", it is the mixture of some of the switching devices, DC-link capacitor and a single DC source completes the part of level generation. The H-bridge in the proposed structure produces the polarity generation part. A detailed explanation of the modulation system and operating modes of the proposed framework are discussed. Finally, in the MATLAB/SIMULINK platform, the projected network topology is simulated and the outcomes are presented.

Corresponding Author:

Abhilash Tirupathi
Department of Electrical and Electronics Engineering
Accendere Knowledge Management Services, CL Educate Ltd., India
Email: abhilash.tripuathi@accendere.co.in

1. INTRODUCTION

Single-phase DC-AC converters are predominant in several industrial and household applications like lathe machines, centrifugal pumps, uninterrupted power supplies, etc. Multilevel single-phase DC-AC converters are highly attractive than two-level inverters due to the advantages of higher power rating, improved power quality and higher reliability. In this context, cascaded converters are highly flexible and modular in the family of multilevel inverters. In this group, "cascaded H-bridge (CHB)" converters [1]-[4] are the classical and traditional types. CHB converters have the advantages of equal voltage stress in symmetrical configurations, easy to add/remove the H-bridges to increase/decrease the voltage levels in the output. MLI technology is spreading to several areas such as AC drives, static reactive compensators, micro-grid systems and renewable energy sources [5]-[8]. The "Flying capacitors clamped (FCC)", "neutral point clamped (NPC)" and "CHB converters" [9]-[11] are established as normal topologies in the MLI family. In this configurations, the device count increases exponentially in reference to the increased in the voltage levels of output. The requirement of unequal voltage ratings of the clamping diodes, unequal capacitor size and a greater number of dc sources puts limitations on these topologies. Several new MLI configurations with the intention of avoiding the drawbacks in the standard topologies were proposed in the literature for several applications [12]-[16]. In recent times, cascaded converters are attracting attention from industries as well as

academia. Several such voltage source inverters (VSIs) were proposed in the literature by employing several combinations of switches, dc power supplies [17]-[20].

In this configuration, the converter has fewer components and lower blocking voltage across the switching devices, resulting in lower costs. The remain papers are organised as; section 2 describes the operating models, section 3 describes the modulation principles that is used to produced the essential "output voltage waveforms", section 4 describes the simulation results that were obtained for different kinds of modulation indices that were used to validate the proposed converter, and section 5 concludes the paper.

2. PROPOSED INVERTER

The recommended converter is depicted in Figure 1. It is used in single-phase alternating current output voltage. It is referred to as an inverter. The converter makes use of eight bidirectional switching devices, one direct current source, and three direct current link condensers. Despite the fact that the switching devices are bidirectional, they only block voltage in single route due to the existence of anti-parallel diode in the circuit. The proposed architecture can make use of three different dc sources, which can be attained from battery banks, photovoltaic systems, or rectifier circuit, respectively. Figures 2 (a) and 2 (b) depict the switchings state at negative and positive zero's output voltage crossing, correspondingly. $V_0=0^+$ known as positive zero-crossing output voltage. $V_0=0^-$ represents an output voltage with a negative zero-crossing voltage. All switches are subjected to the same amount of switching states in order to maintain a increased temperature.

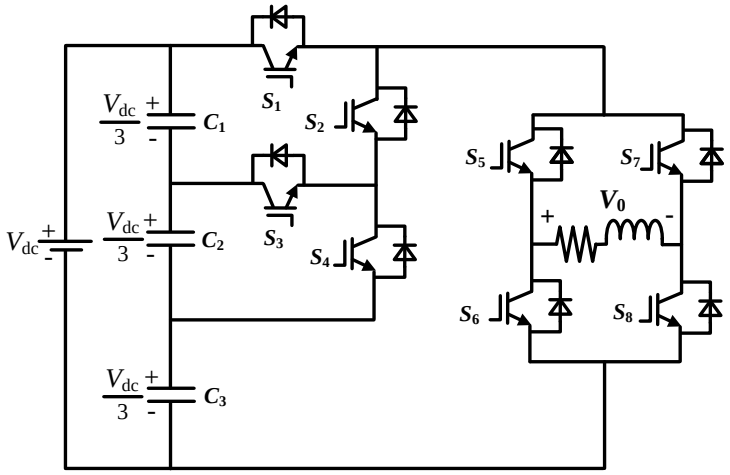


Figure 1. Schematic diagram of the proposed module

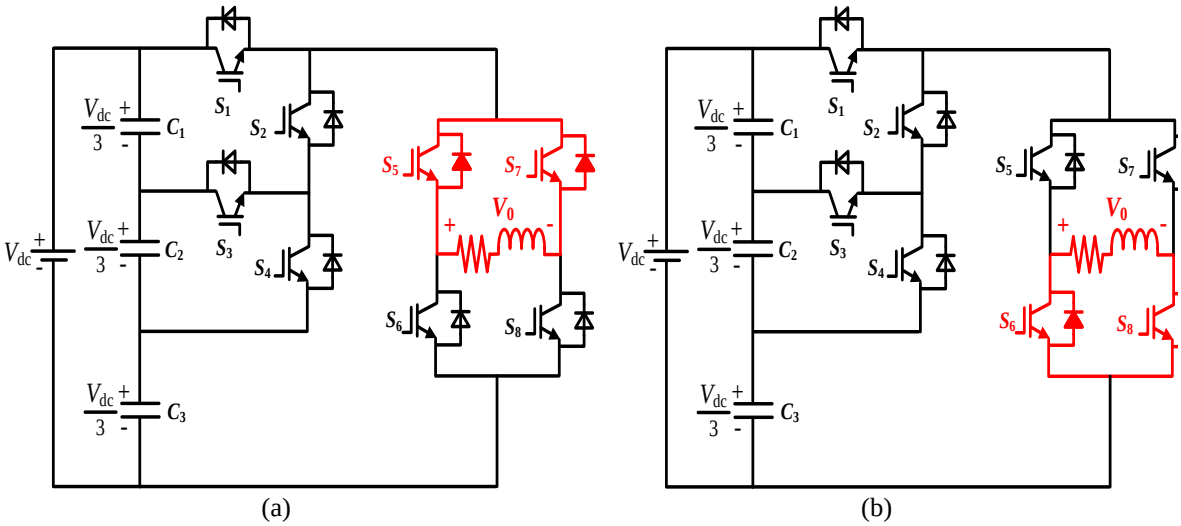


Figure 2. Operating methods through zero crossing: (a) $V_0=0^+$, (b) $V_0=0$

Figure 3 represents the process of the projected converters to produce a positive levels voltage transversely to the output's terminal. Figure 3 (a) generated $V_0=V_{dc}/3$, in this working modal, the control semiconducting material used in devices for IGBTs S_2, S_4, S_5 and S_8 conduct. Figure 3 (b) produces $V_0=2V_{dc}/3$, in these operating modes, the IGBTs S_2, S_3, S_5 and S_8 conduct. Figure 3 (c) shown the peak's voltage of $V_0=V_{dc}$, in these operating modes, the IGBTs S_1, S_5 and S_8 manner. The working methods of the converters used to croped the adverse output voltages levels are shown in Figure 4. Figure 4 (a) generated $V_0=-V_{dc}/3$, in these operating models, the IGBTs S_2, S_4, S_6 and S_7 turn on. Figure 4 (b) provides the output voltage $V_0=-2V_{dc}/3$, during this period the IGBTs S_2, S_3, S_6 and S_7 turn on. Figure 4 (c) stretches the output voltages $V_0=-3V_{dc}$, throughout these periods the IGBTs S_1, S_6 and S_7 turn on.

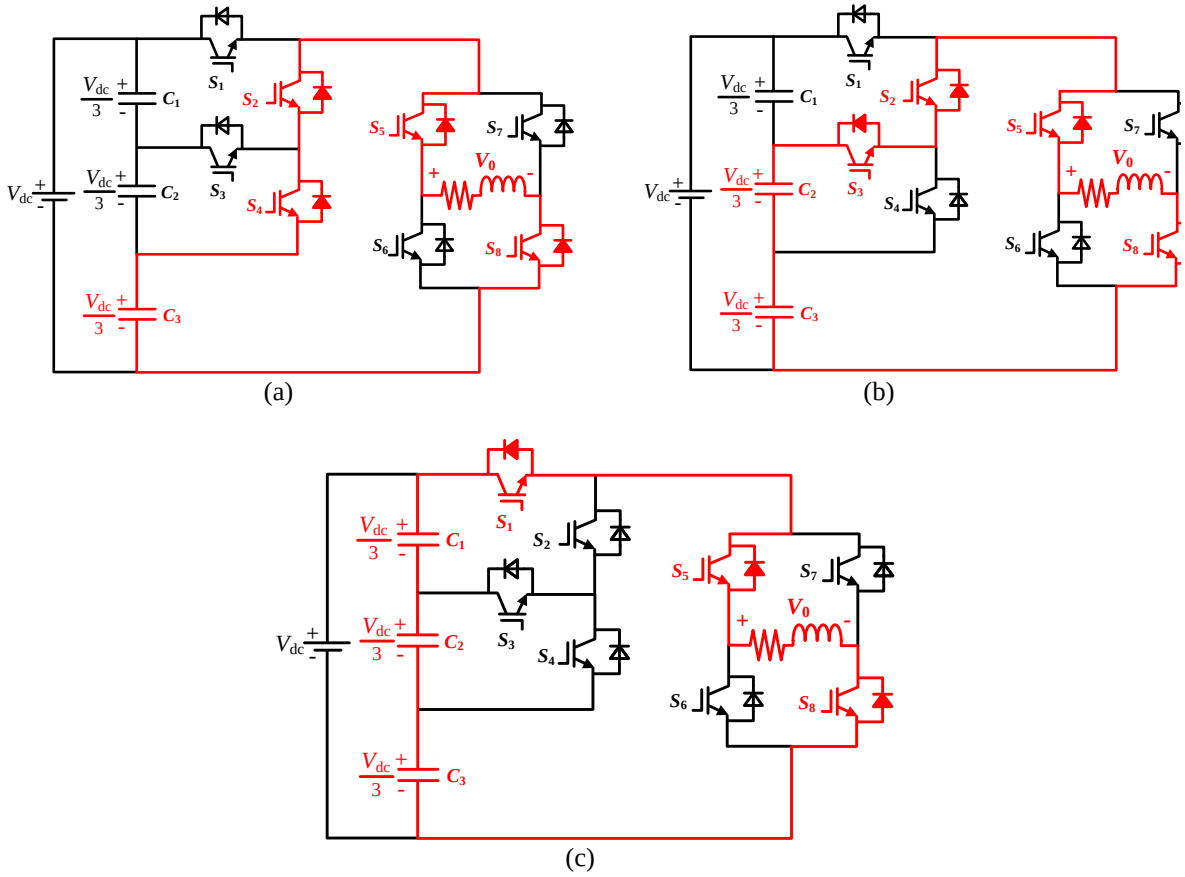


Figure 3. Positive-level working methods, (a) $V_0=V_{dc}/3$, (b) $V_0=2V_{dc}/3$, (c) $V_0=V_{dc}$

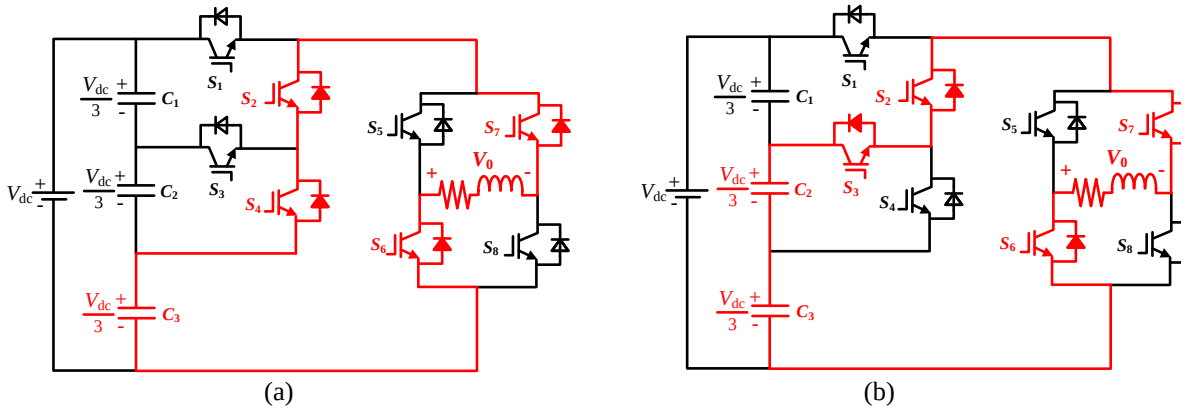
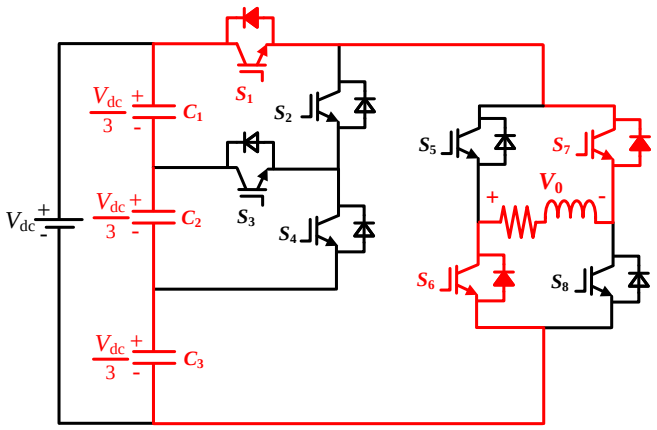


Figure 4. Operating methods through negative voltage level, (a) $V_0=-V_{dc}/3$, (b) $V_0=-2V_{dc}/3$



(c)

Figure 4. Operating modes during negative voltage levels, (c) V_0=-V_{dc} (*continue)*

3. MODULATION TECHNIQUE

In order to make it easier to describe Table 1 shows the switch states at numerous output voltage in the proposed converter, while showing the switch states at several output voltage in the proposed converter. The digits 1 and 0 are used to signify the on and off states of the IGBTs in Figure 1, as shown in the accompanying table: Table 1 the switches are all correctly positioned. S_5, S_6, S_7 and S_8 are better due to their lower switching frequencies. Figure 5 shows the modulation technique [21]-[23]. The concept will use it to create a gate pulse for IGBTs in the suggested system. Six triangular waveforms are used to produce a pure sinusoidal waveform. Both the sinusoidal wave and the triangular wave are known as reference and carrier waves, respectively. The reference waves interact with each carrier wave at specific time intervals, 1, 2, 3, 1', 2', and 3'. This explains why the subsequent pulses are P1-P3 and N1-N3. The output voltage is generated by logical gate circuits that efficiently use these pulses. The total number of output levels is based on the modulation index (M.I.), that is described as:

$$M.I. = \frac{V_{0peak}}{3 \times V_{dc}} \quad (1)$$

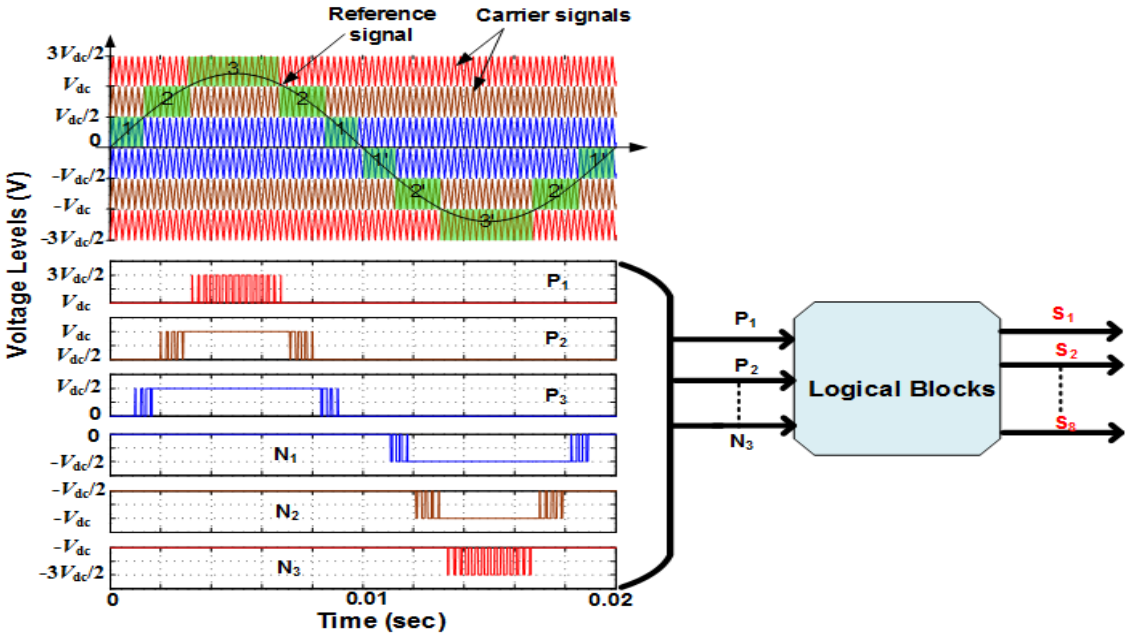


Figure 5. Sine-triangle comparison method

Table 1. Inverter switching sequence

Output voltage level (V_0)	S1	S2	S3	S4	S5	S6	S7	S8
V_{dc}	1	1	0	1	0	0	0	1
$2V_{dc}/3$	0	1	1	0	0	0	0	1
$V_{dc}/3$	0	1	0	1	1	0	0	1
0^+	0	0	0	0	1	0	1	0
0^-	0	0	0	0	0	1	0	1
$-V_{dc}/3$	0	1	0	1	0	1	1	0
$-2V_{dc}/3$	0	1	1	0	0	1	1	0
$-V_{dc}$	1	0	0	0	0	1	1	0

4. SIMULATION RESULTS

The reproduction parameters [24], [25] are meant to result in an output voltage of 230 V and a frequency of 50 Hz, respectively. Table 2 contains a list of the extra parameters that will be considered in the simulation. The waveforms of the inverter current and output voltage for an M.I. of 0.9 and 0.6 are shown in Figures 6 (a) and 7 (a), respectively, for the inverter current and output voltage. For example, Figures 6 (a) and 7 (a) show the respective outputs voltage waveforms with currents, with the former representing seven levels and the latter representing five levels, respectively. As a result, when the M.I. is reduced, the peak voltage of the output will decrease as well. (V_{0peak}). Figures 6 (b) and 7 (b) show the FFT spectrums of the inverter output voltage at various levels of M.I., respectively. V_{0peak} It can be seen that 323 V is modulated at the inverter at a rate of 0.9, with a entire harmonics distortion of 22.4%. This is illustrated in Figures 6 (b) and 7. The decreased in M.I. leads to an increased in THD by reducing the numbers of 'output voltage level,' which is understandable in Figures 6 (b) and 7 (b).

Table 2. Configuration parameters

Parameters	Values
V_{dc}	240 V
P_{output}	732 W
V_0	236 V
I_0	4.9 A
Switching frequency (f_{sw})	4 kHz
Fundamental frequency (f_m)	50 Hz

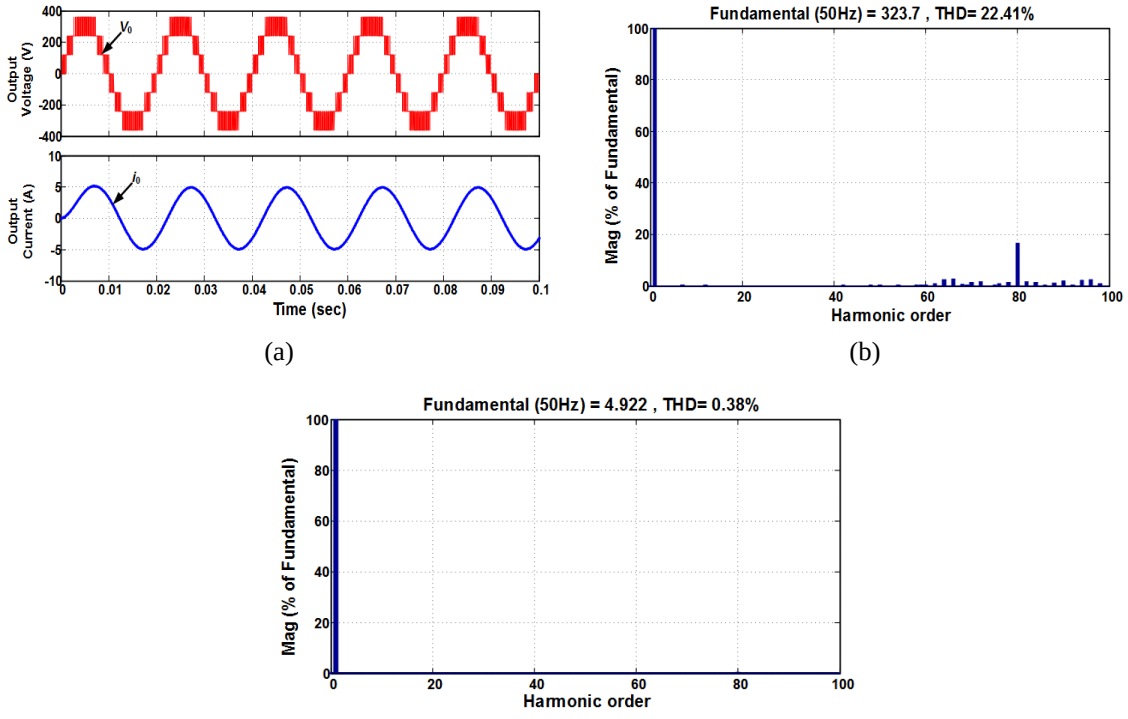


Figure 6. Simulink result of the converters at *M.I.=0.9;* (a) converters voltage and current waveforms at the output, (b) FFT spectrum of V_0, (c) FFT analysis of I_0

Figures 6 (c) and 7 (c) represents each harmonics spectrum of the present output waveforms. At 0.9, the values of I0 peak is 4.9 A, whereas the total harmonic distortion (THD) is roughly 0.4%. The value of I0peak decreases in response to the voltage reductions in M.I. The amount of I_{0peak} is disgunished as 3.2 A and the THD is around 0.6%. Figure 8 depicts the performance of the shown in configuration to withstand the sudden changes in load. It can be observed in Figure 8 that the projected techniques is effective. The circuit can be produced the undistorted output w.r.t changes in the load.

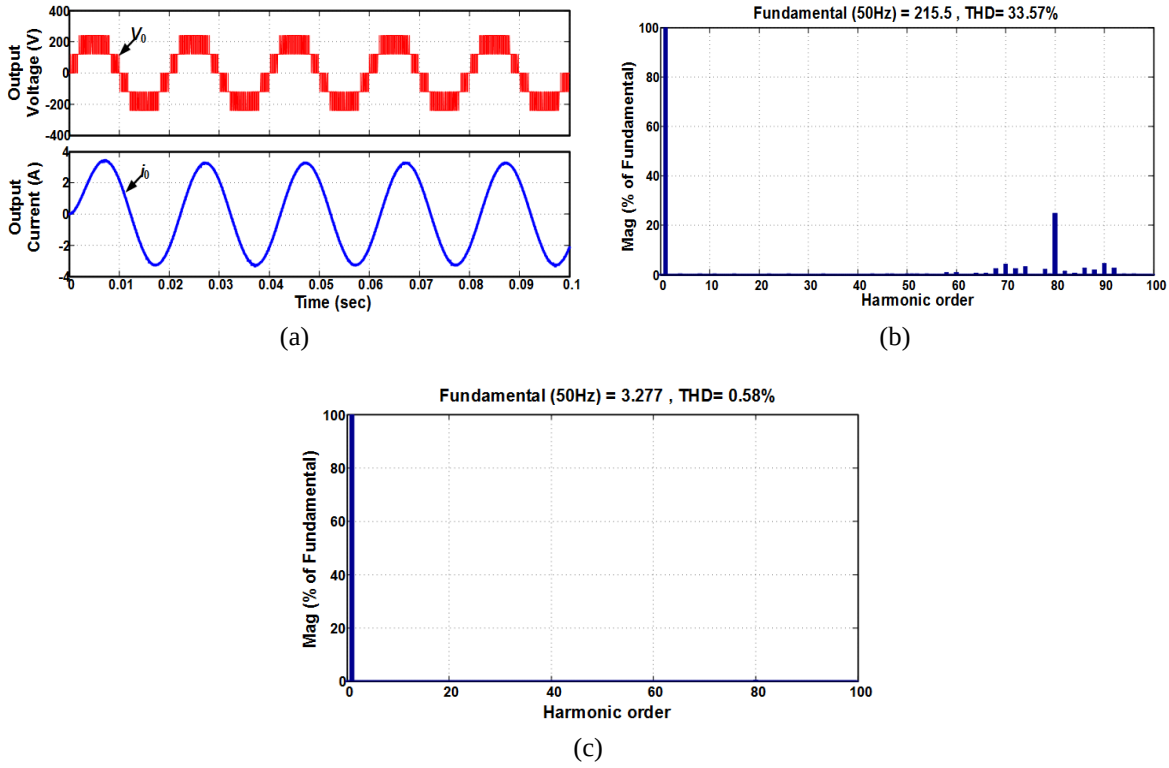


Figure 7. Simulink result of the converters at M.I.=0.62; (a) converters voltage and current waveforms at the output, (b) FFT spectrum of V0, (c) FFT analysized of I0

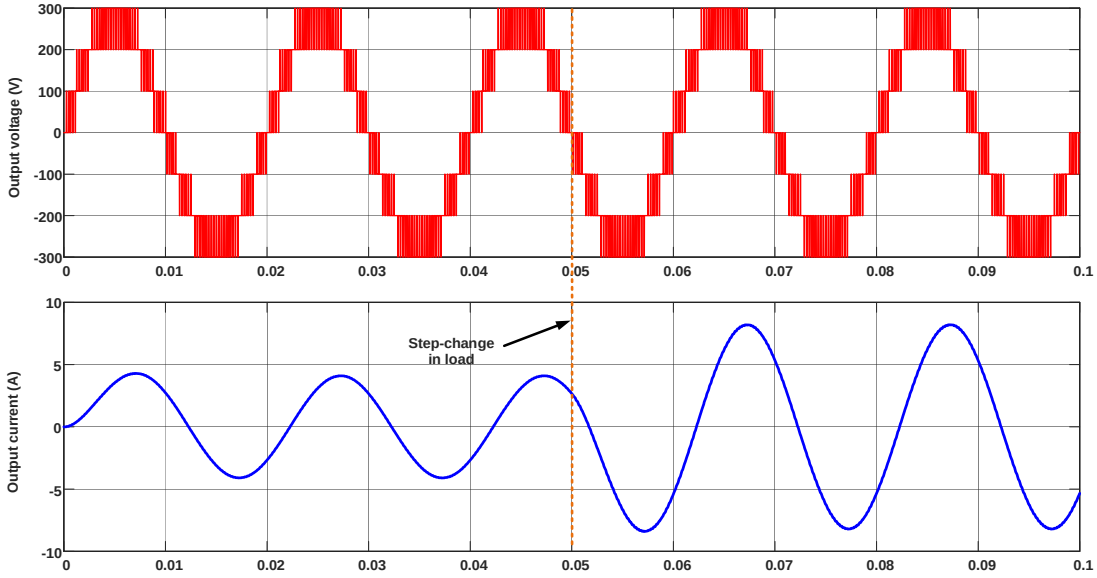


Figure 8. Dynamic responsed of the proposed formation for a step-change in load at m_a=0.9

5. CONCLUSION

This article features the simplified DC-AC MLI configuration. When it comes to creating the requisite number of output voltage levels for the inverter while employing the fewest number of components possible, a tri-tier circuit and an H-bridge are the most efficient methods available. The analyses and operating modes that were used to achieve zero, positive, and negative levels were discussed in depth in order to achieve these results. Without regard to the fundamental frequency, H-bridge switches in the projected network topology have a "lower switching frequency" when compared to other switches. With the suggested architecture, switching losses are more controlled, and as a result, total efficiency is increased. A sinusoidal PWM approach generates the firing pulses required by employing the most efficient technique available at the time. The findings of the MATLAB/SIMULINK system have been confirmed for MI of 0.9 and 0.6, correspondingly. As can be observed from the FFT output spectrum, the THD in the waveforms of the system meet with the IEEE 1547 standard.

REFERENCES

[1] S. Szuba, "An approach to the design of energy storage reactors for DC-to-DC switching power converters using ferrite structures," in *IEEE Transactions on Magnetics*, vol. 16, no. 5, pp. 1271-1278, September 1980, doi: 10.1109/TMAG.1980.1060798.

[2] P. R. K. Chetty, "CIECA: Application to Current Programmed Switching Dc-Dc Converters," in *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-18, no. 5, pp. 538-544, Sept. 1982, doi: 10.1109/TAES.1982.309266.

[3] S. Raghavendran, K. S. Kumar, A. Tirupathi and C. B, "An Improved Three-level DC-DC Boost Converter for Renewable energy Systems with High Gain," *2020 3rd International Conference on Energy, Power and Environment: Towards Clean Energy Technologies*, 2021, pp. 1-6, doi: 10.1109/ICEPE50861.2021.9404467.

[4] A. Tirupathi, K. Annamalai and S. V. Tirumala, "A three-phase inverter circuit using half-bridge cells and T-NPC for medium-voltage applications," *International Journal of Circuit Theory and Applications*, vol. 48, no. 10, pp. 1744-1765, 2020, doi: 10.1002/cta.2833.

[5] H. Matsuo and F. Kurokawa, "New Solar Cell Power Supply System Using a Boost Type Bidirectinal DC-DC Converter," in *IEEE Transactions on Industrial Electronics*, vol. IE-31, no. 1, pp. 51-55, Feb. 1984, doi: 10.1109/TIE.1984.350020.

[6] C. T. Rim, G. B. Joung and G. H. Cho, "Practical switch based state-space modeling of DC-DC converters with all parasitics," in *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 611-617, Oct. 1991, doi: 10.1109/63.97759.

[7] T. Abhilash, A. Kirubakaran and V. T. Somasekhar, "A novel three-phase seven-level inverter," *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*, 2017, pp. 1-5, doi: 10.1109/IPACT.2017.8245146.

[8] T. Abhilash, A. Kirubakaran and V. T. Somasekhar, "A Seven-Level Hybrid Inverter with DC-Link and Flying Capacitor Voltage Balancing," *2019 IEEE International Conference on Environment and Electrical Engineering and 2019 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2019, pp. 1-5, doi: 10.1109/EEEIC.2019.8783553.

[9] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," in *IEEE Transactions on Industry Applications*, vol. 35, no. 5, pp. 1098-1107, Sept.-Oct. 1999, doi: 10.1109/28.793371.

[10] T. Abhilash, K. Annamalai and S. V. Tirumala, "A Seven-Level VSI With a Front-End Cascaded Three-Level Inverter and Flying-Capacitor-Fed H-Bridge," in *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6073-6088, Nov.-Dec. 2019, doi: 10.1109/TIA.2019.2933378.

[11] B. Wang, X. Zhang and H. B. Gooi, "An SI-MISO Boost Converter With Deadbeat-Based Control for Electric Vehicle Applications," in *IEEE Transactions on Vehicular Technology*, vol. 67, no. 10, pp. 9223-9232, Oct. 2018, doi: 10.1109/TVT.2018.2853738.

[12] R. Wai, C. Lin, R. Duan and Y. Chang, "High-Efficiency DC-DC Converter With High Voltage Gain and Reduced Switch Stress," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 354-364, Feb. 2007, doi: 10.1109/TIE.2006.888794.

[13] M. D. Manjrekar, P. K. Steimer and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," in *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 834-841, May-June 2000, doi: 10.1109/28.845059.

[14] X. Yuang, H. Stemmler and I. Barbi, "Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 256-263, 2001.

[15] C. Restrepo, J. Calvente, A. Cid-Pastor, A. E. Aroudi and R. Giral, "A Noninverting Buck–Boost DC–DC Switching Converter With High Efficiency and Wide Bandwidth," in *IEEE Transactions on Power Electronics*, vol. 26, no. 9, pp. 2490-2503, Sept. 2011, doi: 10.1109/TPEL.2011.2108668.

[16] K. Kruse, M. Elbo and Z. Zhang, "GaN-based high efficiency bidirectional DC-DC converter with 10 MHz switching frequency," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 273-278, doi: 10.1109/APEC.2017.7930705.

[17] A. Tsunoda, Y. Hinago and H. Koizumi, "Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 4011-4021, Aug. 2014, doi: 10.1109/TIE.2013.2286559.
[18] J. Wu and C. Chou, "A Solar Power Generation System With a Seven-Level Inverter," in *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3454-3462, July 2014, doi: 10.1109/TPEL.2013.2279880.
[19] M. A. Hutabarat, S. Hasan, A. H. Rambe and S. Suherman, "Design and simulation hybrid filter for 17 level multilevel inverter," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 9, no. 3, pp. 886-897, 2020, doi: 10.11591/eei.v9i3.890.
[20] C. Kannan and C. K. Kishore, "A comparison of three phase 27 level inverter scheme under no load and multiple load conditions," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 3, no. 4, pp. 245-250, 2014, doi: 10.11591/eei.v3i4.302.
[21] T. Abhilash, A. Kirubakaran and V. T. Somasekhar, "A New Structure of Three-Phase Five-Level Inverter With Nested Two-Level Cells," *International Journal of Circuit Theory and Applications*, vol. 47, no. 9, pp. 1435-1445, 2019.
[22] T. Abhilash, A. Kirubakaran and V. T. Somasekhar, "A new hybrid flying capacitor based single phase nine-level inverter", *International Transactions on Electrical Energy Systems*, vol. 29, no. 12, pp. 1-15, 2019.
[23] L. S. H. Priya, K. Rajesh, U. Satya Sai Polaraju and N. Rajesh, "Simulation and Analysis of Seven-Level Voltage Source Inverter," *Soft Computing Techniques and Applications*, Springer, Singapore, vol. 1248, pp. 111-120, 2020, doi: 10.1007/978-981-15-7394-1_10.
[24] C. R. Balamurugan and K. Vijayalakshmi, "Comparative analysis of various z-source based five level cascaded H-bridge multilevel inverter," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 7, no. 1, pp. 1-14, 2018, doi: 10.11591/eei.v7i1.656.
[25] R. Saravanan and P. S. Manoharan, "Power Quality Improvement Using Unified Power Quality Conditioner Based on Particle Swarm Optimization," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 2, no. 1, pp. 29-34, 2013, doi: 10.11591/eei.v2i1.259.