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A cascaded converter using hybrid cells and H-bridge structure

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ABSTRACT

This paper introduces a cascaded converter structure using hybrid two-level cells to form a single-phase seven-level inverter. Compared to various conventional and existing multilevel (MLI) topologies, this topology requires a lower number of devices. It uses several DC sources integrated in two-stage cells to provide the required voltage. In this topology, the DC-link condensers are not necessary. The modes of operation and modulation of the structure proposed are described in depth. Finally, in the MATLAB/Simulink platform the new topology is evaluated and the results reported.

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1. INTRODUCTION

Cascaded converters are highly flexible and modular in the family of multilevel inverters. In this group cascaded H-bridge (CHB) converters [1]-[3] are the classical and traditional types. CHB converters have the advantages of equal voltage stress in symmetrical configurations and easy to add/remove number of output voltage levels can be reduced or increased using H-bridges. MLI technology is spreading to several areas such as AC drives, static reactive compensators, micro-grid systems and renewable energy sources [4]-[6]. The standard topologies in the MLI family include the neutral point clamped (NPC), flying capacitor clamped (FCC), and CHB converters [7]-[10]. In these configurations, the device count increases exponentially w.r.t the number of levels in the output voltage, the requirement of unequal voltage ratings of the clamping diodes, unequal capacitor size and a greater number of dc sources puts limitations on these topologies. Several new MLI configurations with the intention of avoiding the drawbacks in the standard topologies were proposed in the literature for several applications [11]-[13]. In recent times, cascaded converters are attracting attention from industries as well as academia. Several such voltage source inverters (VSIs) were proposed in the literature by employing several combinations of switches, dc power supplies [14]-[17].

In this design, the converter seems to have the benefits of reducing the number of components and lowering the limiting voltage throughout the switching devices. The rest of the section is arranged as follows: the operating principle and working is presented in section; the modulation techniques is described in section 3 for generating the appropriate voltage waveform. The presented converter is verified with simulation

results for various modulation indices in section 4 and in section 5 represents the conclusion part of the presented paper.

2. SYSTEM CONFIGURATION

Figure 1 shows the presented converter and It is essentially a single-phase, seven-level voltage inverter with AC output. The converter has ten bidirectional switches and three DC sources, each of which is isolated. While bi-directional conducting qualities do exist in switching devices, anti-parallel diodes render the voltage impossible to transmit in the opposite direction. Three distinct dc sources can be used in the proposed topology: battery banks, PV systems, or rectifier circuits.

The switches in the positive and negative zero output voltage transitions are shown in Figures 2 (a) and 2 (b). $V_0=0^+$ V0+ is a designation for the output voltage at the zero-crossing of a positive cycle and the output voltage is at $V_0=0^-$ when the machine passes through the zero-crossing point. The switch S_2 can be used to produce the zero-voltage level. By turning-on, the switches S_2, S_4, S_6, S_7 and S_{10} the voltage across the output is zero. But this mode is not shown in the figures. In case of any requirement, this operating mode can be utilized to produce the zero-voltage level. For temperature control, the switching levels should be the same in each switch, and the use of both states should be equal.

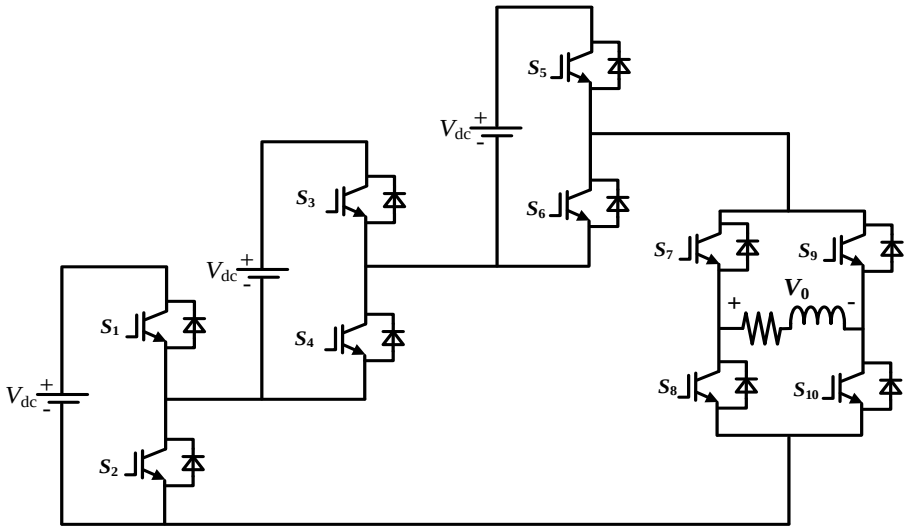


Figure 1. Proposed conver schematic layout

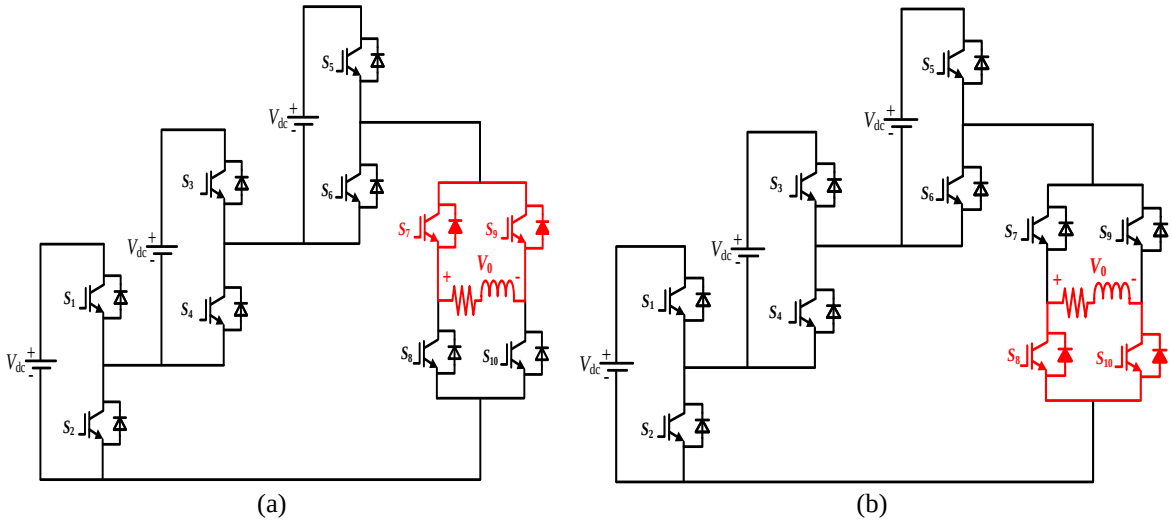


Figure 2. At zero crossing; (a) $V_0=0^-$, (b) $V_0=0^+$

Figure 3 shows the converter's output terminals receiving a positive voltage from the converter, which is depicted in the following diagram and in Figure 3 (a) represents at $V_0=V_{dc}$, herein functional method of the power semiconductor devices (IGBTs) S_1, S_4, S_6, S_7 and S_{10} conduct is given. Figure 3 (b) generates $V_0=2V_{dc}$, and the IGBTs S_1, S_3, S_6, S_7 and S_{10} conduct. Figure 3 (c) is shwon the peak voltage of $V_0=3V_{dc}$, in this operating mode, the IGBTs S_1, S_3, S_5, S_7 and S_{10} conduct. Figure 4 shows the working modes of the converter that provide negative output voltage levels. Figure 4 (a) shows volatage level at $V_0=-V_{dc}$ and in this condistion, the IGBTs S_1, S_4, S_6, S_8 and S_9 turn on. Figure 4 (b) shows the voltage level at $V_0=-2V_{dc}$ and in this situation, the IGBTs S_1, S_3, S_6, S_8 and S_9 turn on. Figure 4 (c) shows the voltage level at $V_0=-3V_{dc}$ and in this condistion, the IGBTs S_1, S_3, S_5, S_8 and S_9 turn on.

Positive voltage levels V_{dc}, $2V_{dc}$ and $3V_{dc}$ and ccur in the output voltage in regions 1, 2 and 3 respectively, as shown in Figure 5 (a). Negative voltage levels $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$ occur in the output voltage in regions 1', 2' and 3' respectively, as illustrated in Figure 5 (a).

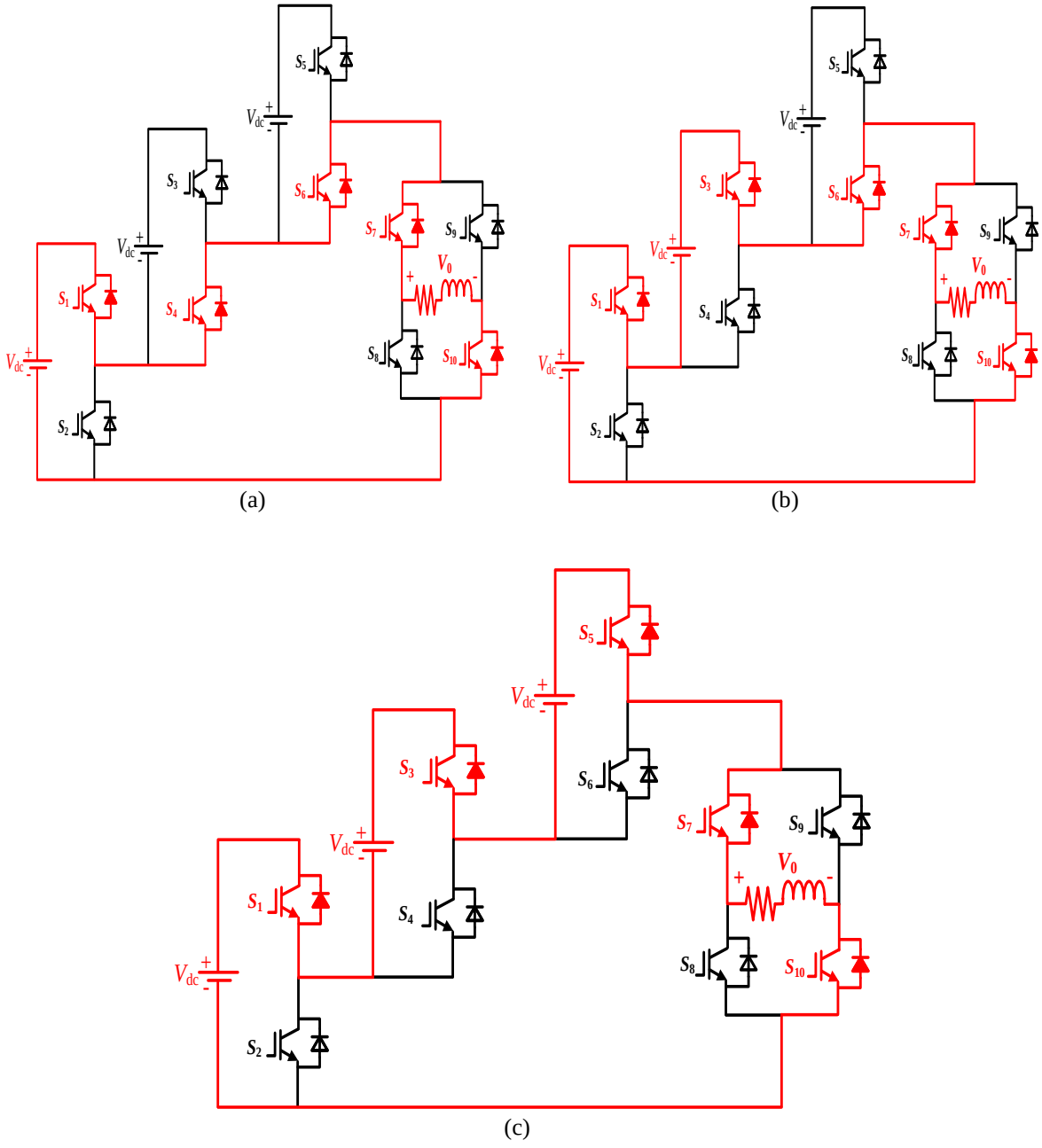


Figure 3. Positive-level operating modes; (a) $V_0=V_{dc}$, (b) $V_0=2V_{dc}$, (c) $V_0=3V_{dc}$

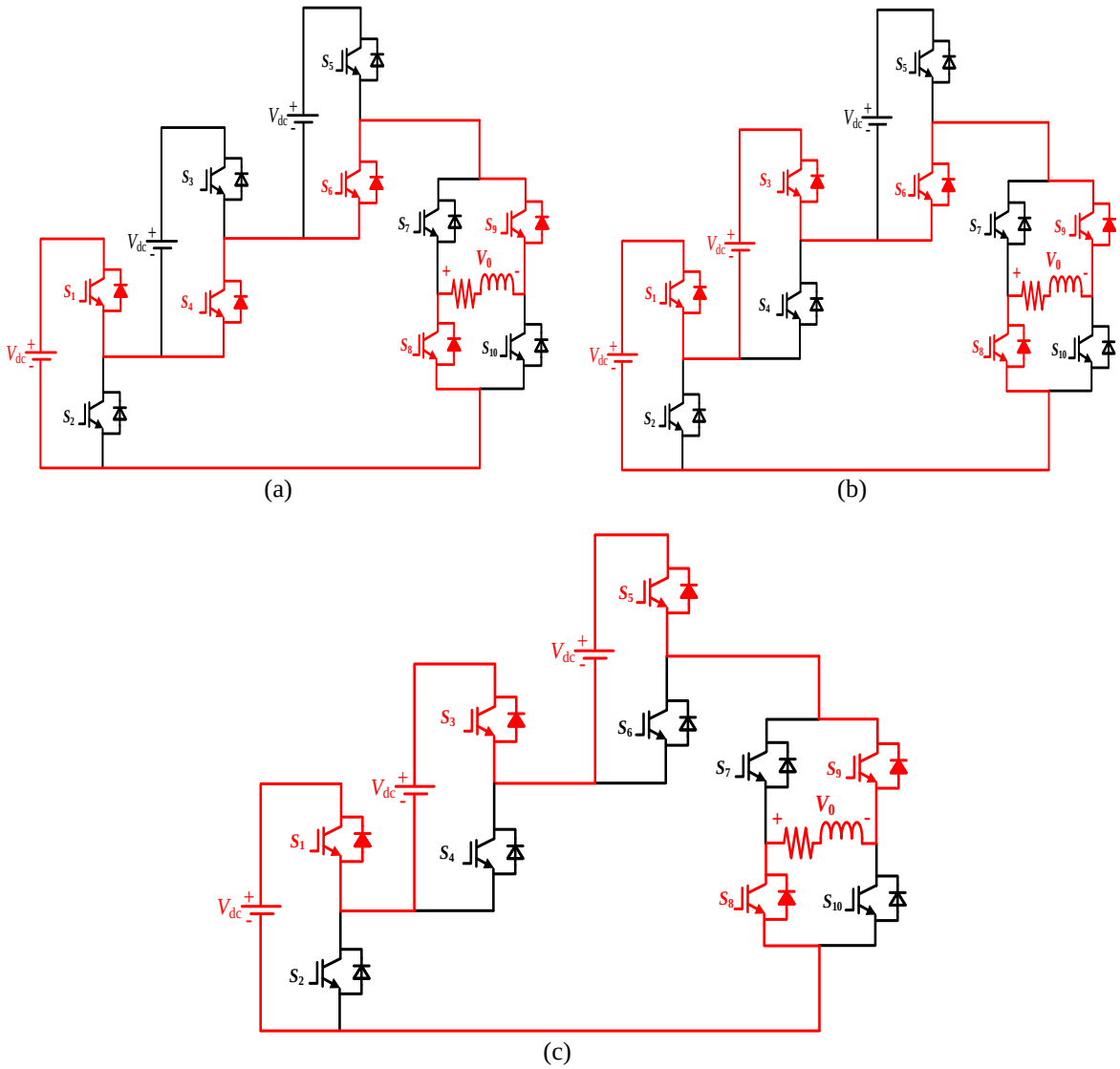


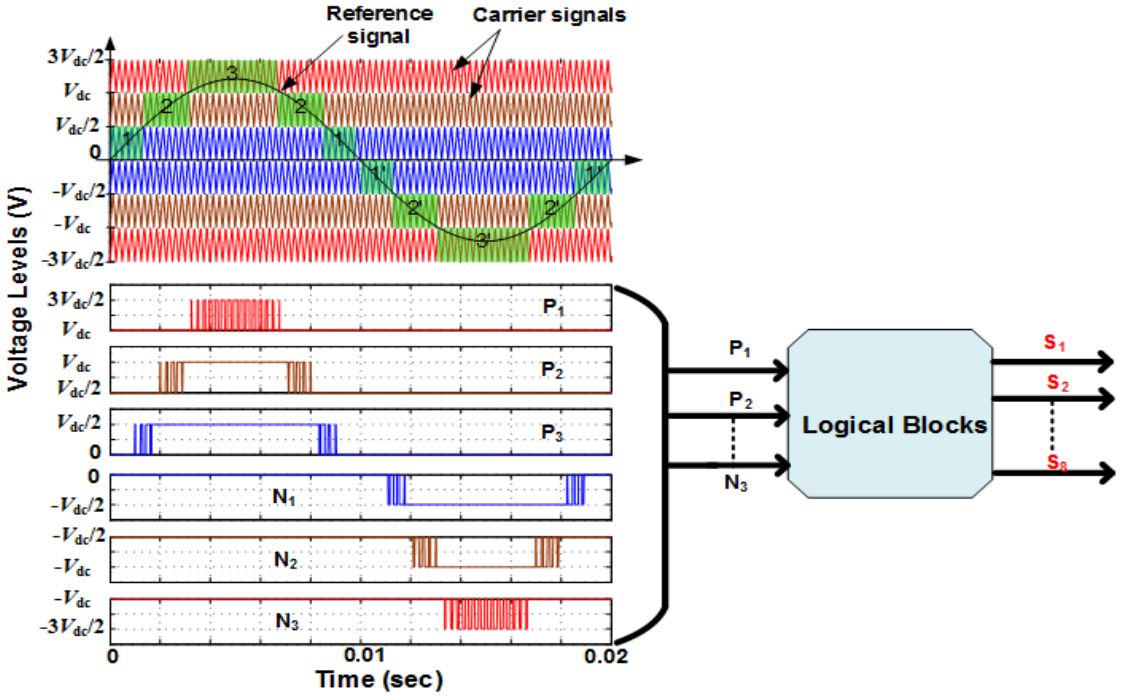
Figure 4. Output when volatage is negative; (a) V_0=-V_{dc}, (b) V_0=-2V_{dc}, (c) V_0=-3V_{dc}

3. MODULATION TECHNIQUE

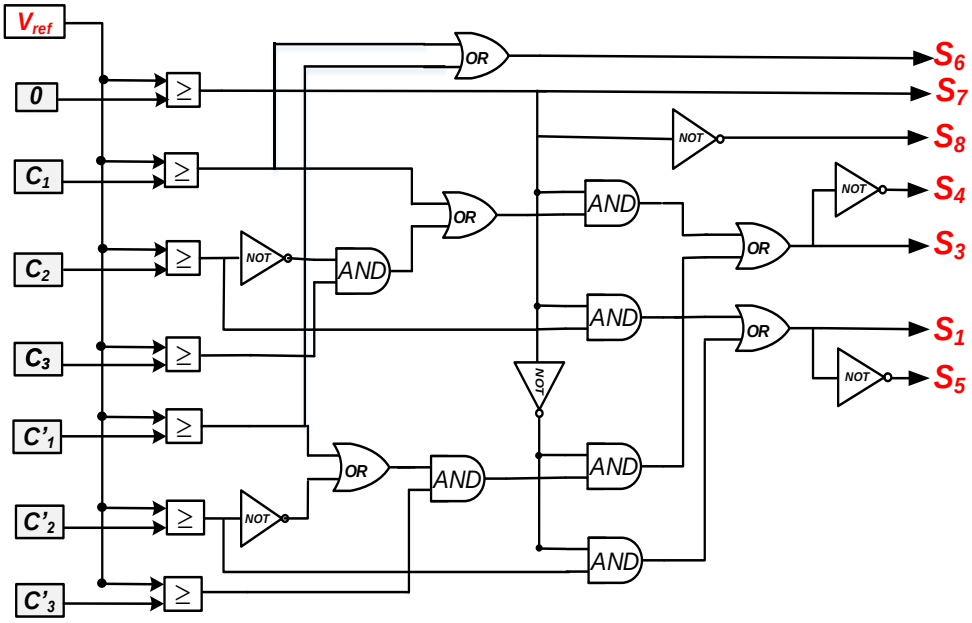
To improve the accuracy of the switch states' descriptions, Table 1 was created to represent the various off and on modes of the switching in the presented converter, according to the output voltage. The IGBTs' on and off modes are represented by the numbers 1 and 0 in Table 1 of Figure 1. The switches S7, S8, S9, and S10 appear to be working at lower switching frequencies, which, in turn, means fewer switching losses.

The modulation technique used for IGBT gate pulse generation in the proposed topology is shwon in Figure 5 (a) [18]-[20] and the logical mapping for the needed inverter pulses to generate 7-L outputs is shown in Figure 5 (b). A single pure sine wave, which is replicated on six triangular waveforms, is added to the overall waveform. A reference wave, which is also known as a sinusoidal wave, is distinguished from a carrier wave, which is also known as a triangle wave. The reference wave is continually being intercepted by all the carrier waves, which are interrupted at 1, 2, 3, 1', 2', and 3'. The result is pulses P1-P3 and N1-N3 due to the connections between both the carrier and reference waves. The requisite seven-level output voltage is created using logical gate circuits that efficiently utilise these pulses. The modulation index (M.I.) for the number of output levels is defined as indicated in [21]:

$$M.I.= \frac{V_{0peak}}{3\times V_{dc}} \quad (1)$$



(a)



(b)

Figure 5. Show, (a) sine-triangle comparison method, (b) logical diagram for gate pulse generation

Table 1. Inverter switching table

Output Voltage Level (V_0)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
$3V_{dc}$	1	0	1	0	1	0	1	0	0	1
$2V_{dc}$	1	0	1	0	0	1	1	0	0	1
V_{dc}	1	0	0	1	0	1	1	0	0	1
0^+	0	0	0	0	0	0	1	0	1	0
0^-	0	0	0	0	0	0	0	1	0	1
$-V_{dc}$	1	0	0	1	0	1	0	1	1	0
$-2V_{dc}$	1	0	1	0	0	1	0	1	1	0
$-3V_{dc}$	1	0	1	0	1	0	0	1	1	0

The comparison chart of the proposed configuration w.r.t several other configurations is shown in Table 2. It can be observed that the proposed topology does not demand any diodes, capacitors and inductors. Hence, the voltage drops and voltage ripples are less in the proposed circuit.

Table 2. Comparison chart

Devices	[11]	[12]	[13]	[14]	[15]	[16]	[17]	[18]	Proposed
Switches	12	12	12	12	10	8	10	10	10
Diodes	--	--	--	--	--	--	--	--	--
Flying capacitors	2	2	2	1	1	1	--	1	--
DC-link capacitors	2	2	--	2	2	2	--	2	--
Inductors	--	--	--	--	--	--	3	--	--
DC Voltage Sources	1	1	1	1	1	2	1	1	3
Total No. of Devices	17	17	15	16	14	13	14	14	13

4. SIMULATION RESULTS

The output voltage is believed to be 230 V and 50 Hz, according to [22]-[24]. In Table 3, the other parameters whose values are important for simulation work can be seen. The waveforms for the inverter output current and voltage in Figures 6 (a) and 7 (a) show M.I. values of 0.9 and 0.6, respectively. Output voltage waveforms for levels 1 through 7 with the appropriate current are depicted in Figure 6 (a), whereas outputs for levels 1 through 5 with corresponding current are presented in Figure 7 (a) [25]. The peak voltage of the output is known to decrease as the motor intensity (M.I.) is lowered (V_{0peak}). The FFT spectra of the inverter output voltage are shown in Figures 6 (b) and 7 (b) at different levels of M.I. The inverter's THD when the modulation is set at 0.9 and 22.4 %, the V_{0peak} is observed as 323 V. The output current waveform's harmonic spectra can be seen in Figures 6 (c) and 7 (c). The THD and modulation from our experiments was measured at 0.4% and 0.9, respectively, with an I_{0peak} of 4.9 A. In line with the voltage, the I0peak value drops in proportion to the M.I. reduction. The THD is roughly 0.6 percent, and the I_{0peak} is 3.2 A.

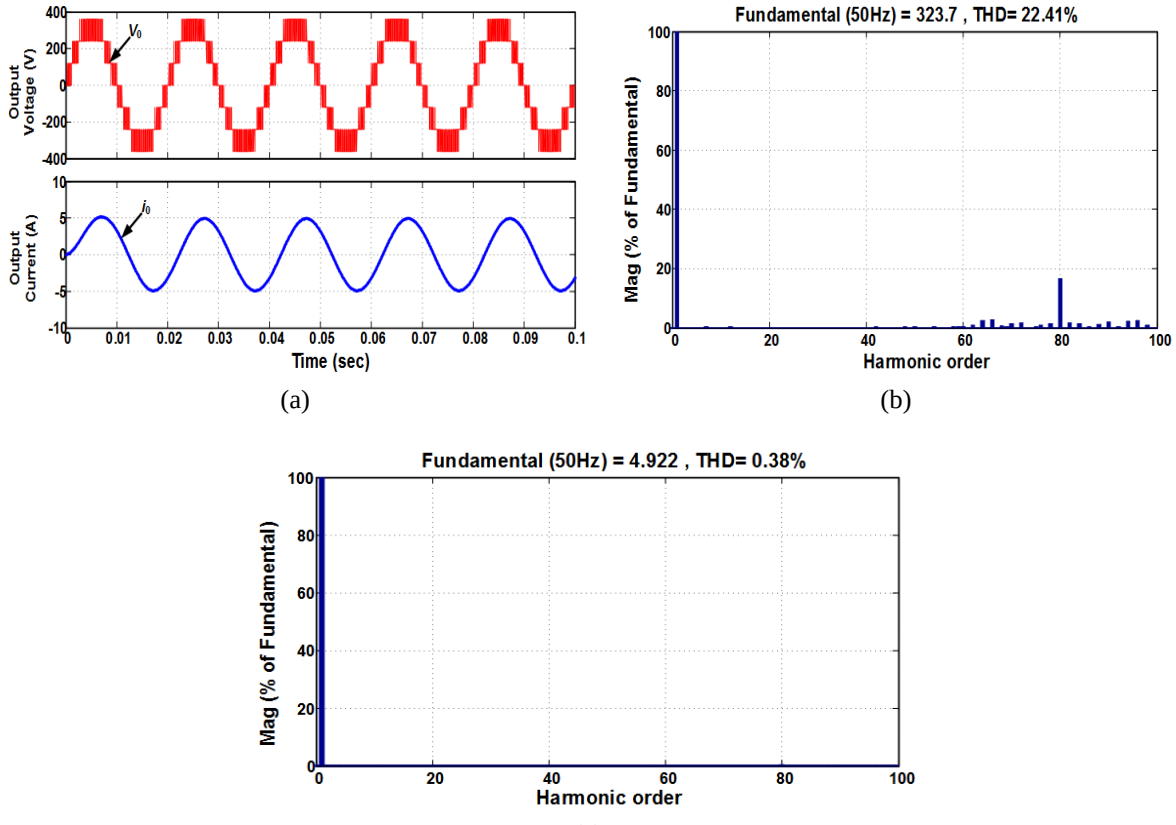


Figure 6. These figures are; (a) converter current and voltage graph, (b) FFT spectrum of V_0, (c) FFT investigation of I_0 at M. I.=0.9

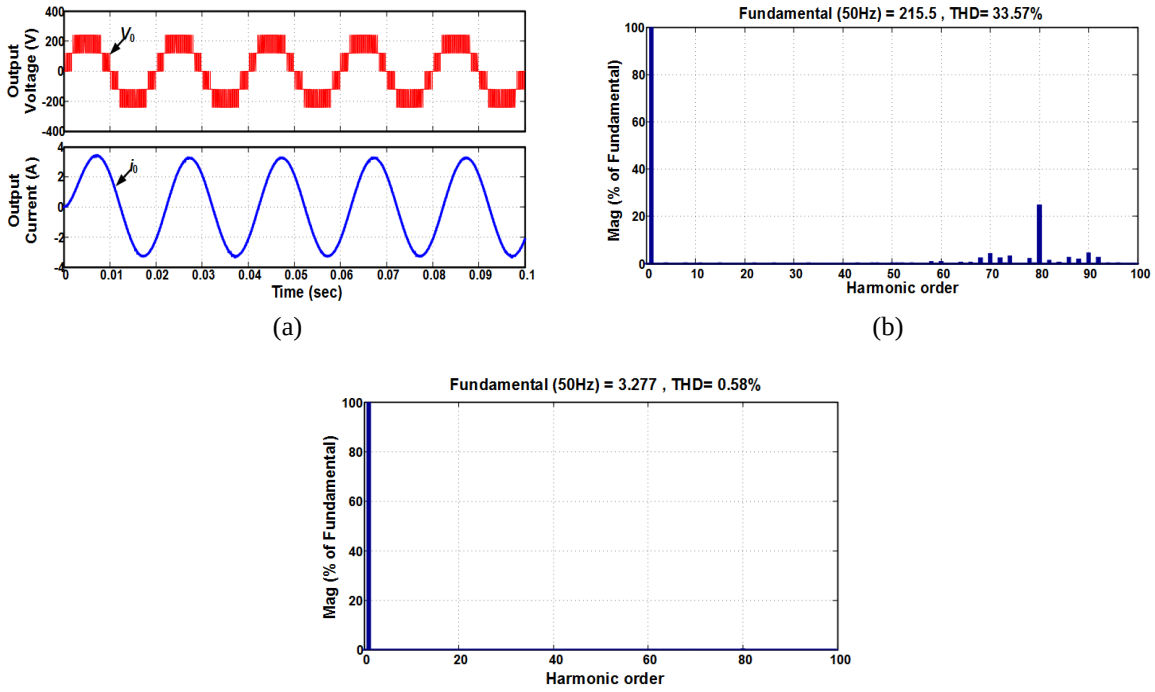


Figure 7. These figures are; (a) converter current and voltage graph, (b) FFT spectrum of V_0, (c) FFT investigation of I_0 at M. I.=0.6

Table 3. Configuration parameters

Parameters	Values
V_{dc}	240 V
P_{output}	730 W
V_0	230 V
I_0	4.9 A
Switching frequency (f_{sw})	4 kHz
Fundamental frequency (f_m)	50 Hz

5. CONCLUSION

A new MLI architecture is addressed in this article. The proposed design is a cascaded double-tier cell combination with an H-bridge that has been used to optimise the number of inverter configurations. The combination has been the most effective combination in recent years. There have been extensive analyses of modes of operation for zero, positive and negative levels. In the suggested topology the H-Bridge switches work at a lower frequency, which corresponds to the fundamental frequency. As a result, the configuration's switching losses are comparatively smaller than various MLI configurations and thus improve the efficiency of the system presented. In order to generate the required firing pulses, the most efficient and least complex sinusoidal PWM technique has been used. The configuration results for MATLAB/Simulink will be validated at 0.9 and 0.6 modulation indexes. FFT output voltage spectrum and output current showing the THD waveform content within the specified limits are indicated.

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