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An intelligent digital low voltage power factor optimizer

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ABSTRACT

In this paper, an intelligent digital low voltage power factor optimizer has been built. This power factor optimizer operates according to the measurement the value of phase shift angle between both of current and voltage, thus the power factor has been measured. It is simply that it will improve the power factor through connecting a set of shunt capacitors in order to reach to an optimal value of the power factor (close to unity). The proposed intelligent digital power factor optimizer for low voltage is built and simulated using the software which is called electronic work bench package (EWB) Multisim. Finally, this optimizer presents a good result when applied to different loads and variable currents. This optimizer is feasible, affordable and ready to be implemented especially in countries that suffer from higher prices of electrical power.

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1. INTRODUCTION

In recent years, the cost of electrical energy has become expensive, as especially in countries that have suffered from wars. The best solution to save electricity is to improve the power factor, thus there will be less consumption of electrical power. Consequently, less cost to the consumer, particularly consumers who seek the help of commercial electricity [1, 2].

The electric power transmission system is very influenced by the value of the current consumed by the various loads, because any increase in current means an increase in the value of losses due to the resistance of the transmission lines. Moreover, most loads are inductive, which leads to decrease the power factor [3, 4]. Some loads like power electronic loads as example, produce harmonic currents and voltages. Thus, this phenomenon leads to increase the losses and decrease of power factor, thus reduction in the efficiency of whole the system. [5].

The procedure that injects reactive elements to make the power factor closer to the unity value is called power-factor correction (PFC) [6]. In order to obtain a power factor very closed to unity, it must be reduced the distortion and losses in voltage, ensure that there is no any reactive power, and required a lowest value of current. This will lead to an increase in the efficiency of the system and reduce the financial costs borne by the consumer [7-10]. Both of improvement the power factor and efficiency of the transmission of power and for a long time was achieved by means of shunt capacitor containing in passive compensator. Relatively the Shunt capacitors are of low cost in respect with maintaining and installing. Using of the shunt capacitor in load zone leads to more stability in voltage [11-15].

There are various types of analog converters, which can be applied to PFC such as canonical switching cell (CSC), CUK converter, Zeta converter [13, 16]. Power factor correction in switched-mode power supply (SMPS) is executed by an analog controller as conventional way. the wide production of digital devices that possesses high performance and lower cost like microprocessors, digital signal processors (DSP)

and field programmable gate arrays (FPGA), induced competition by implementing digital controller of SMPS [17-19]. Furthermore, an intelligent power factor correction based on artificial neural networks (ANN) is introduced a simple and low-cost solution for power factor compensation [20]. Some techniques have advantages like simplicity and to control large amount of power economically [11, 21]. All the current process of digital PFC controller takes analog laws base on them. There is a similarity between the digital PFC and analog systems in the algorithm of average current mode control [5]. There are many advantages for the digital controller over the analog one like increasing in reliability, ability to the systems reproduction, sensitivity of noise is less, higher algorithms complexity, and the monitoring of signals will be easy [4].

A new approach of power factor correction is presented here, which is the intelligent digital low voltage power factor optimizer. This optimizer operates based on the measurement of the phase displacement angle between both of current and voltage, and then improves the power factor to the optimal values (close to unity) by connecting the array of shunt capacitors. Designing the intelligent digital circuit of this optimizer is the aim of this paper [22].

2. THE PROPOSED POWER FACTOR OPTIMIZER

It is typically for the power factor optimizer to perform with twice of loops which are internal fast current loop in order to obtain closed to unity power factor, second the external slow voltage loop for the output voltage stabilization [4, 23]. The proposed power factor optimizer depends on the measuring of displacement between the AC voltage and AC current. This angle determines the value of the power factor, whenever the value of the phase angle is decreasing the value of the power factor will increase according to (1) in [7, 24].

$$PowerFactor = \cos\theta \quad (1)$$

where θ :is the displacement between current and voltage waves.

The power factor optimizer placed between the AC power supply and the load as shown in Figure 1. This optimizer calculates the displacement between current and voltage waves through converters the voltage and current waves to square wave, and then calculates the phase shift duration time between them. The phase angle will be measured according to phase shift duration time by the digital counter. The digital counter will start of counting with begin of this time and stop counting when the time is ending. The counter frequency is 18 KHz because the frequency of power supply is 50 Hz, and each cycle is 360 degrees, so each phase angle degree has time equal to (1/18 KHz) [8].

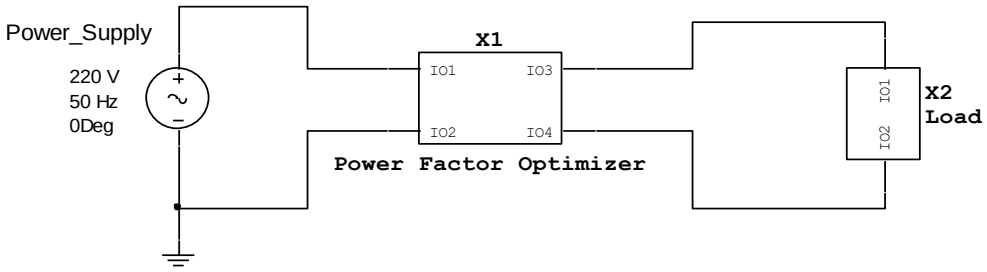

Figure 1. Power factor optimizer system

When the phase angle is greater than the certain value (the desired value to make the power factor closed to unity) the optimizer will connect the first shunt capacitor to decrease the phase angle. Thereafter, the optimizer will measure the phase angle again and connect the anther shunt capacitor to reduce this angle, and so on. The proposed optimizer finished shunt capacitor connection when the power factor reached to desired value or greater than it. Figure 2 illustrates the block diagram of the proposed power factor optimizer [25].

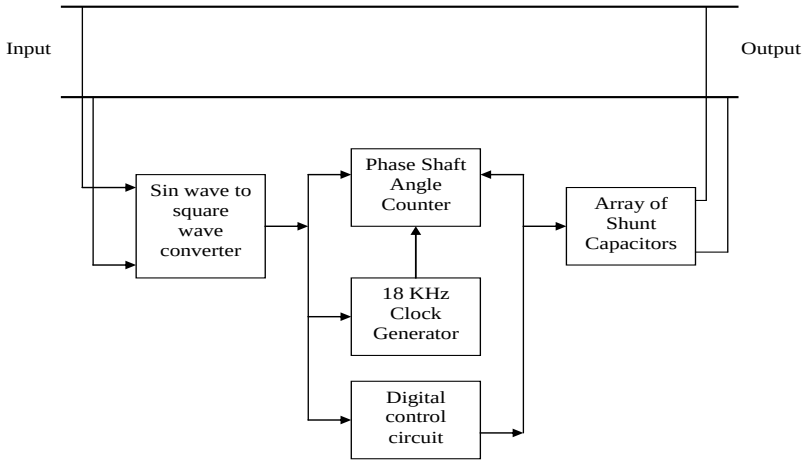

Figure 2. Power factor optimizer block diagram

3. THE INTELLIGENT DIGITAL POWER FACTOR OPTIMIZER

The intelligent digital low voltage power factor optimizer is designed as shown in Figure 3 and test using electronic work bench (EWB) Multisim simulator.

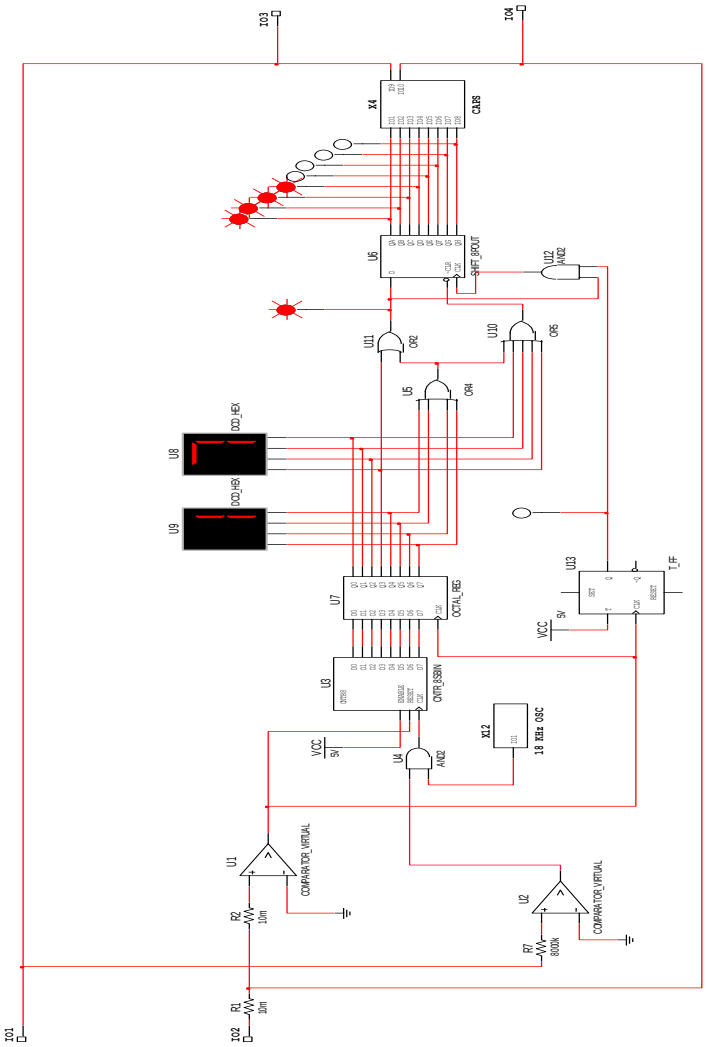

Figure 3. The proposed design of intelligent digital power factor optimizer

The operational amplifiers U1 and U2 operate as a zero-crossing detector to convert the voltage and current to half square wave as shown in Figure 4, thus the phase shift duration time can be calculated between them. A very small resistor R1 is placed in series with the input power supply so it will be possible to produce the current wave. This resistance is the very small value so as to be no effect on the value of the source voltage.

An 8-bit counter U3 is used to count the duration time between the voltage and current waves, which represent the phase shift angle. The clock of the counter is generated by the 8 KHz oscillator X12. Figure 5 illustrates the electronic circuit of the 8 KHz oscillator. This oscillator consists of a 555-timer built as a stable operation form.

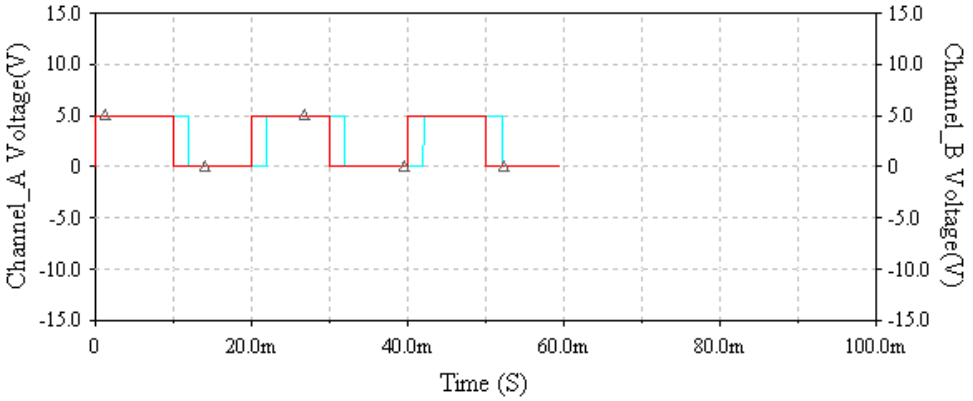

Figure 4. The zero-crossing detector output

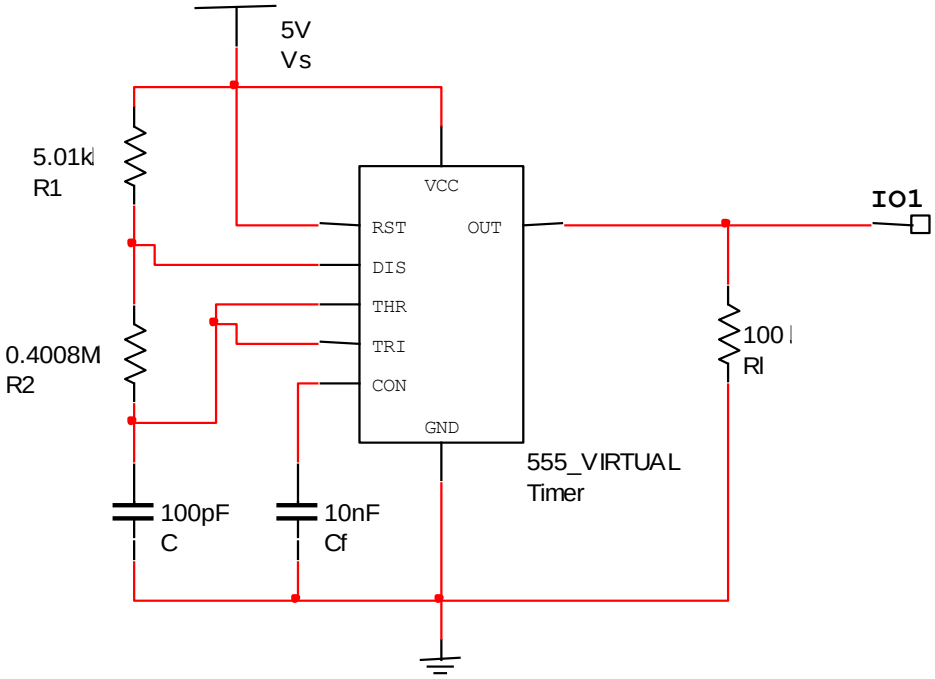

Figure 5. The 8 KHz oscillator

When phase shift duration time is ending the counted number will be transferred to the control digital circuit through the 8-bit PIPO register U7. The digital control circuit (U5, U10, U11, and U12) is responsible for connection the shunt capacitors X4 through SIPO 8-bit register U6 according to the desired power factor. Figure 6 illustrate the array of shunt capacitors is cleared. The dc source Vcc used in this design has been generated from the circuit shown in Figure 7.

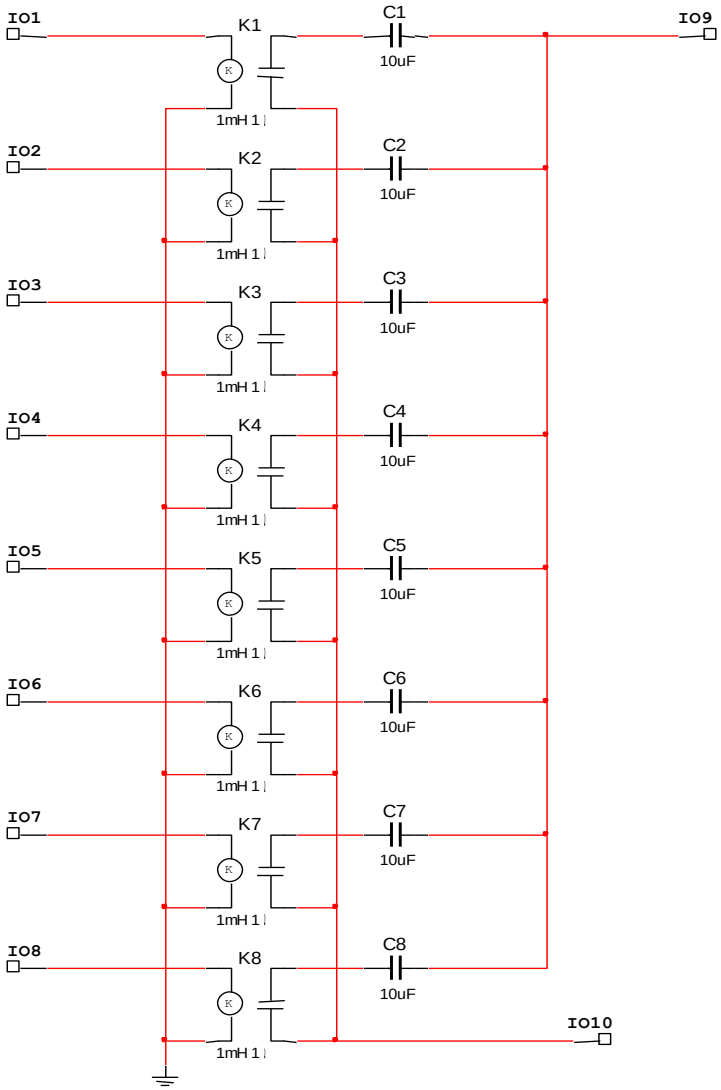

Figure 6. The shunt capacitors array

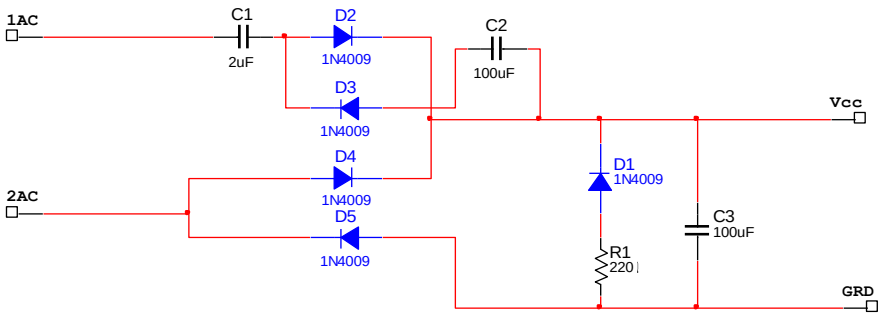

Figure 7. The dc source circuit

The minimum phase angle in this design is 8º so that the power factor will be at least 0.99, which is acceptable for design requirements. Figures 8-10 shows the result when the power factor optimizer tests at constant load (power factor equal 0.8) and 10 Ampere current. As it cleared in Figure 8 the current reduced to 80% of its value after 160 ms. Every 20 ms the shunt capacitor connected in parallel with the load. Furthermore, the power factor is increasing gradually until reach to desired value (close to unity) as shown in Figure 9. Finally, the apparent power is reducing to reach the active power as illustrates in Figure 10.

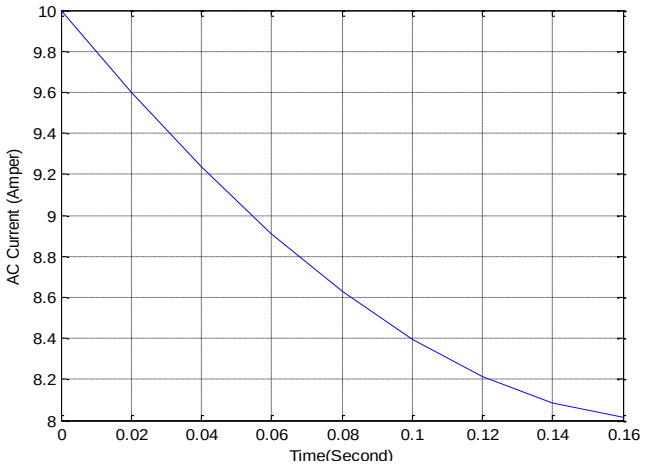

Figure 8. The relationship between the current and the time at constant load

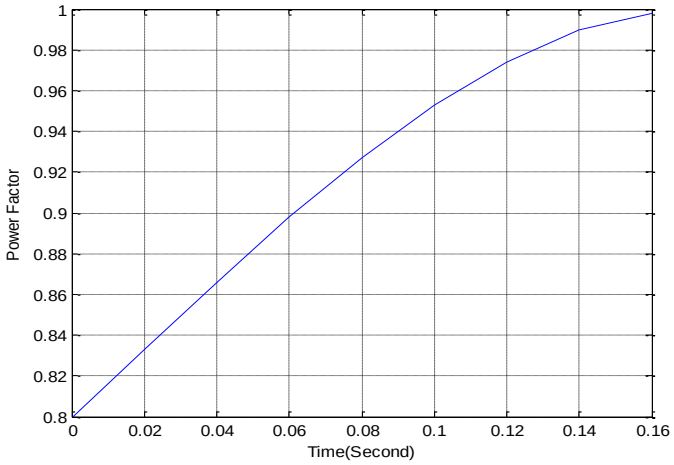

Figure 9. The relationship between the power factor and the time at constant load

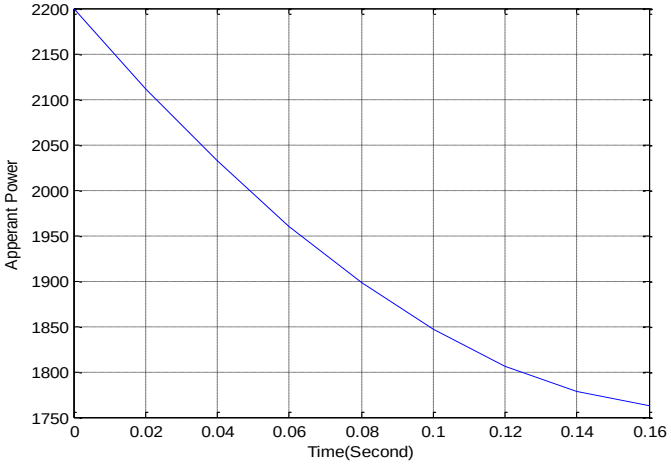

Figure 10. The relationship between the apparent power and the time at constant load

The results shown in Figures 11-13 are appeared when the power factor optimizer is tested at 10 Amperes current and variable load, while Figure 14 is presents when the optimizer is tested at 0.8 power factor and variable current.

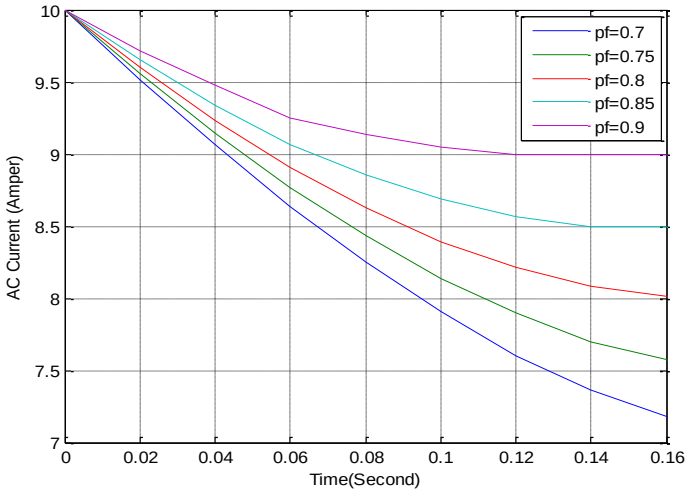

Figure 11. The relationship between the currents and the time at variable load

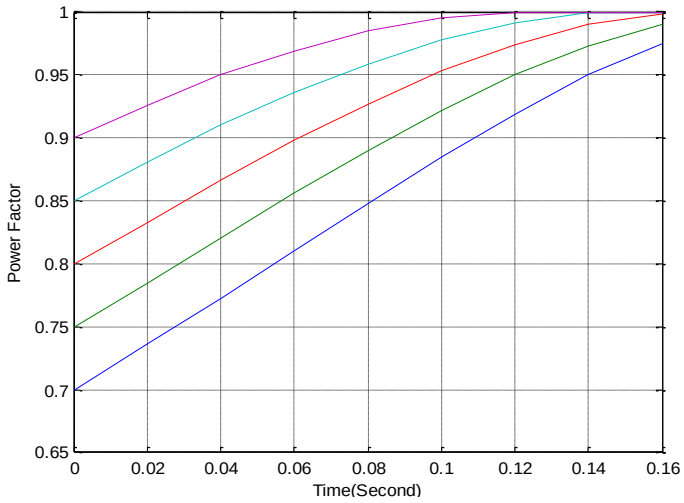

Figure 12. The relationship between the power factors and the time at variable load

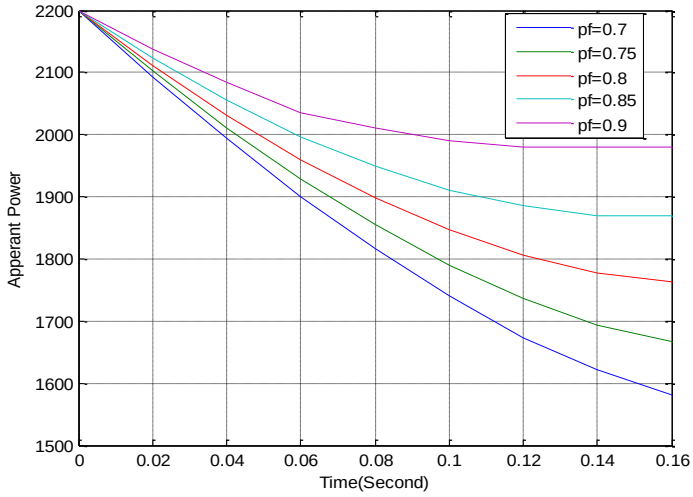

Figure 13. The relationship between the apparent powers and the time at variable load

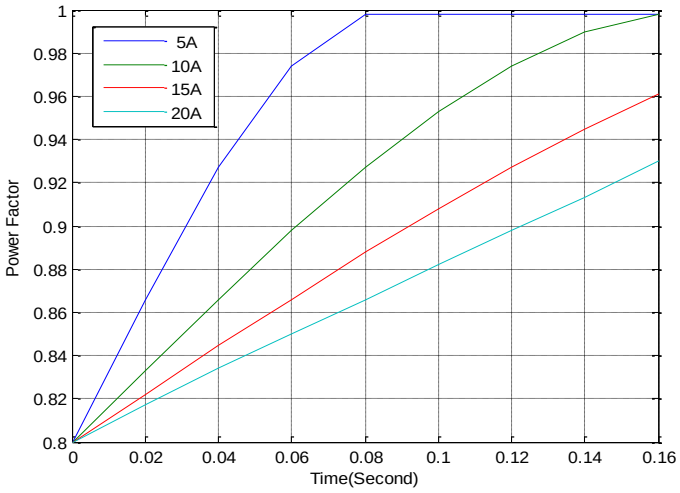

Figure 14. The relationship between the power factors and the time at variable load and current

4. CONCLUSION

Most loads are an inductive load, so there will be a loss of the apparent power and the power factor will reduce. Moreover, the electric power reached to the consumer does not use properly. So, the best solution is using the power factor optimizer to increase the power factor and save the electric power. In this paper, the intelligent digital low voltage power factor optimizer has been presented. The digital power factor optimizer operates according to the phase displacement between current and voltage. This optimizer measures the phase angle and connects the shunt capacitor to reduce the power factor to the desired value. This optimizer can be used in every house in Iraq to reduce the consumer power and save the electrical cost. Especially since this optimizer is cheap because most of the components used are simple, a long-life consumer, do not need to high-energy, and with the capability of repair parts separately.

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