

Single event latch-up detection for nano-satellite external solar radiation mitigation system

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Article Info

Article history:

Received Jun 9, 2016

Revised Nov 20, 2016

Accepted Dec 11, 2016

Keywords:

Cubesat

Electrical power subsystem

Single event effect (SEE)

Single event latch-up (SEL)

Single event upset (SEU)

ABSTRACT

This paper presents the single event latch-up (SEL) detection for nano-satellite external solar radiation mitigation system. In this study, the SEL detection analysis was conducted using circuit test and simulation. An electrical power subsystem (EPS) is a part of all CubeSat bus subsystems and it comprises solar arrays, rechargeable batteries, and a power control and distribution unit (PCDU). In order to extract the maximum power generated by the solar arrays, a peak power tracking topology is required. This may lead to the SEL with the presence of high voltage produced by solar. To overcome the SEL problems, the circuit test and simulation must be done so that the flow of SEL will be easily detected and mitigate. The method that been used are by using microcontroller, the SEL will be created in the certain time. The programable integrated circuit (PIC) are used to mitigate SEL effect. It indicates that, the SEL occur very fast in certain time. When the simulation is conducted by using SPENVIS, the result shows, only single event upset (SEU) was affected on UiTMSAT-1.

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1. INTRODUCTION

On August 10th 2018, UiTMSAT-1 the first UiTM's nanosatellite has successfully made their launch to the space from the international space station (ISS). This BIRDS-2 Cubesat nanosatellite along with the other 2 Cubesats, MAYA-1 from the Philippines and BHUTAN-1 from Bhutan is orbiting in low earth orbit (LEO) at the altitude of approximately 400 km. The nanosatellite is currently orbiting around the Earth with the velocity of 7.66km/s and execute the transmission of its beacon to the UiTM ground station. The UiTM ground station is situated at the Faculty of Electrical Engineering, Tower 2, Engineering Complex, UiTM Shah Alam [1-3].

When it comes to LEO path, there are several radiations that is present. This radiation may lead to some single event effect (SEE) which consists of single event upset (SEU), single event-latchup (SEL), single event burnout (SEB), and single event gate rupture (SEGR) [4-9]. This paper is focusing on SEL effects and mitigating it. In complementary metal-oxide-semiconductor (CMOS) technologies or in some silicon on insulator (SOI) when n- and p-type devices are built into common silicon islands, SEL presents in bulk. It has been found in space cosmic ray environments and terrestrial neutron accelerated tests. In addition, SEL may generate non-catastrophic interconnect damage from melting [10-14].

The SEL results in the maneuvering satellite platform (MSP) and programable integrated circuit (PIC) devices in radiation test. Furthermore, it commonly did not result in failed devices although drawing high current. In consequence, there is always a danger of latent failures. Tested MSP devices were found to not operate properly. after $1 \times 10^6/\text{cm}^2$ at $86 \text{ MeV-cm}^2/\text{mg}$ linear energy transfer (LET). On the contrary, devices such as PIC, Atmel, Intel and Qualcomm devices were observed to operate properly (after powder cycle) after exposure to more than $1 \times 10^7/\text{cm}^2$ at LETs of at least $75 \text{ MeV-cm}^2/\text{mg}$. It is crucial to have a stable and reliable power system for a Cubesat to be functioning. The Cubesat will not be able to do anything else without electrical power other than drifting around in orbit. Hence, the EPS subsystem contributes a primary role in this case. The current must be limited to protect the subsystem if the EPS draws a current that is immense enough to suggest a malfunction [15]. The SEL might occur to the spacecraft which is in this case, Cubesat, caused by heavy ion or protons from cosmic rays or solar flares during the operation. Even small increment of current over normal supplied current, the SEL will occur and may damage the systems overall. [16-23].

This paper presents on simulating SEL event by using radiation in substitute of using microcontroller. Also using PIC to detect and mitigate the SEL that occur as replicate to nano-satellite. The objective for this research puts its emphasis on SEL that takes place to the system through the solar panel and collecting the data during normal current and during the SEL occurred. Latch-up is destructive and a power cycle is required to restore the operation. A significant vulnerability in CMOS space systems happens as a result of the latch-up that is stimulated by ionizing radiation such as high-energy proton or heavy-ions from deep space. The sensitivity of an integrated circuit (IC) to SEL relies on assorted process parameters as well as design geometry [24]. Nevertheless, it can be corrected if the SEL is detected and the device's power is quickly turned off, then turned back on. So, the detection of SEL must be detected faster before its occurrence to avoid the harm to the other components. The SEL can take place in split second at any time at certain temperature [25, 26] especially in space. The mitigation of the SEL must be there as well so that the device can operate normally and continue with the main missions without any trouble.

2. RESEARCH METHOD

2.1. Block diagram

Figure. 1 shows that the SEL is occurring in the gray box. This is where the radiation from space with several amount of energy that can cause the SEL effect. The mitigation must be done before the radiation starts to damage the OBC. In this case, the system must be turn off immediately and turn it back on [27]. This is where the reset PIC take place in order to reset the system.

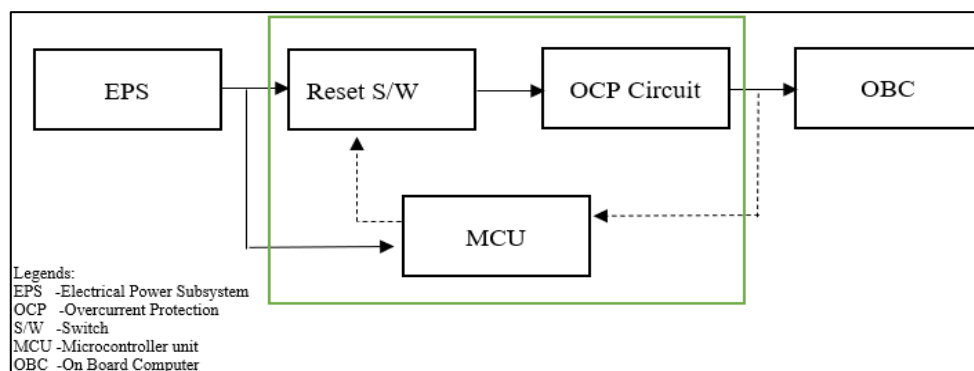


Figure1. Block diagram of reset PIC placed between EPS and OBC

By using PIC16F1787, it may protect the OBC from harm of SEL. It is functioned to reset the systems. The PIC was named as reset PIC. First, the process starts with the normal current supply to the PIC. In this state, there is nothing happened and the flow of current smooth. The current flow straight to the overvoltage protection which is used here is LTC4361CTS81. After a several time, the high current will be injected to the process which is in this case it is equal to SEL occurrence. The overcurrent protection will detect the high current and will reset the flow of the current so that the board is not receive any damage. After a few periods, the process will turn back on and flow the normal current back to the on-board computer. Figure 2 shows the flowchart of mitigating the SEL. While Figure 3 shows the EPS standard block diagram used in this system to analyze the SEL effect in Cubesats.

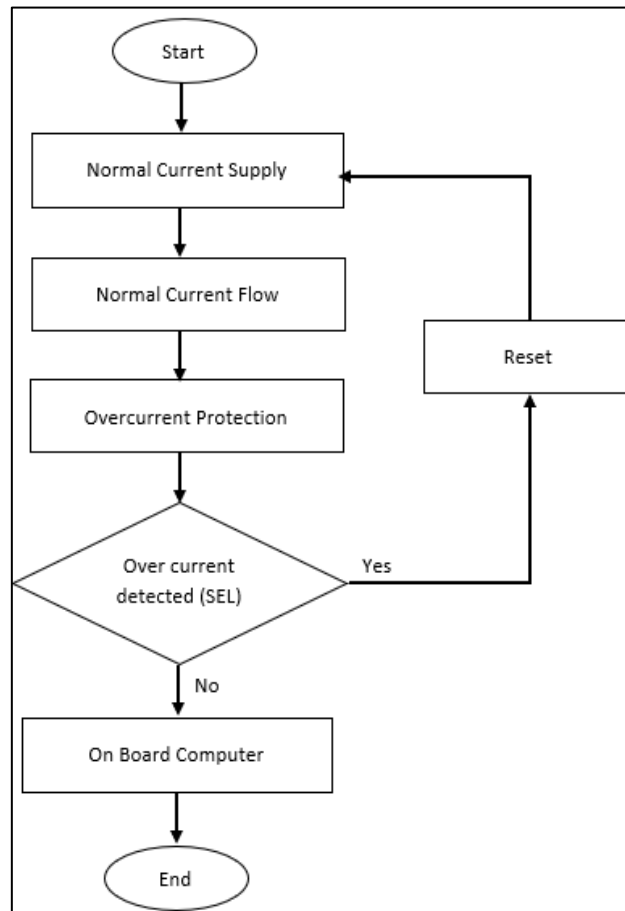


Figure 2. The flowchart of mitigating the SEL

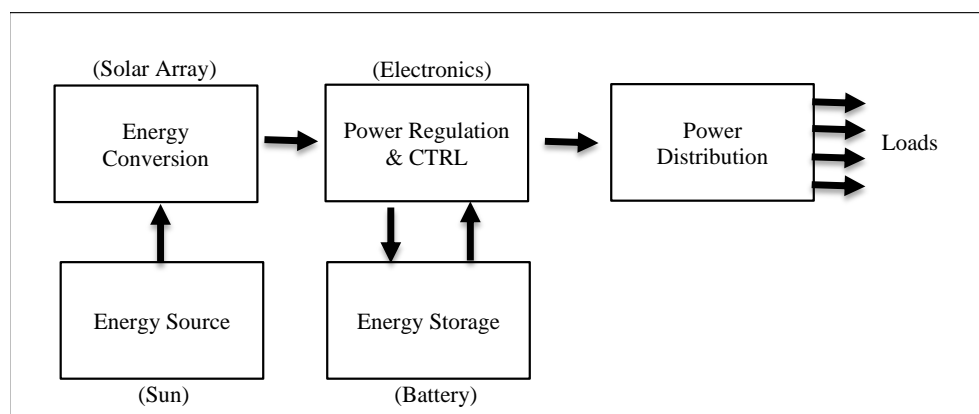


Figure 3. EPS standard block diagram

2.3. Circuit study related to SEL

The latch-up structure can be represented as a circuit behavioral model as shown in Figure 4 [27]. The model includes the junction resistance, the substrate resistance, the well resistance, and two cross-coupled BJTs. This model relies on measured resistance and BJT characterization values to accurately represent latch-up behavior. However, even without the specific resistances, the behavioral model is useful in exploring the effect of the resistor values on latch-up behavior, which is related to the spacing parameters under study in this work.

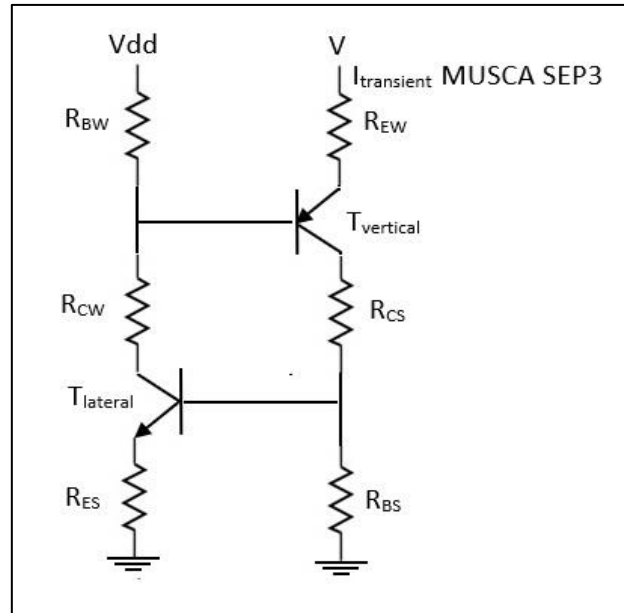


Figure 4. Latchup behavioral circuit model [27]

From model in Figure 4, the critical SEL parameter values for V_{Hold} and V_{Trig} are calculated from (1) and (2):

$$V_{Trig} = V_{DD} - V_{PNPth} \left(1 - \frac{R_{EW}}{R_{BS}} \right) \quad (1)$$

$$V_{Hold} = V_{Trig} - \frac{R_{EW} \left(1 - \frac{R_{EW} R_{ES}}{R_{BS} R_{BW}} \right)}{R_{ES} + R_{CW} + R_{BW}} V_{DD} \quad (2)$$

V_{Trig} requires knowledge of the vertical parasitic bipolar junction transistor (BJT) threshold voltage, V_{PNPth} , well emitter resistance, R_{EW} , and the substrate trigger resistance, R_{BS} . V_{Trig} represents the minimum required voltage to forward-bias the vertical parasitic BJT. V_{Hold} represents the level above which sustains the latch-up phenomenon. It depends on V_{Trig} and a combination of the resistors in the model due to the feedback loop that sustains latch-up behavior [19].

3. RESULTS AND DISCUSSION

3.1. Testing inject current

Figure 5 shows the current increase observed during the proton test when SELs were observed. The three SELs included in this figure were observed at 5200, 5700 and 6000 sec, respectively. Before a SEL, the current consumption was near 40 mA. It jumped to nearly 180 mA at the time of a SEL occurrence (see 5200 sec). The only way to exit from the SEL condition was to turn the power on and off. The SELs were initialized by turning off the power to the test article at 5500, 5900 and 6100 sec, respectively. As the SELs occurred so quickly, it was difficult to see the nominal operation with a 40-mA current before the third SEL due to the limited data sampling rate.

3.2. Spenvis simulation

The testing using Spenvis is to see the activity of SEL in space. This reason why this test is to get the real value of SEL occurrence in real space area. The test has been set with Malaysia's satellite UiTMSAT-1. All kind of radiation effects that can affect the satellites orbiting in LEO are investigated and represented in graphical form with the help of SPENVIS. We know that the radiation exposure of spacecraft in LEO is dependent on orbit inclinations and altitudes, the Figure 6 shows the of ionizing dose for UiTMSAT-1 in its own altitude inclination. The graph shows the ionizing dose effects on the aluminum shielding of the satellite, it also shows that the effect of electrons fades as the thickness of the shielding is increased but on the other hand the effect of proton has not much change.

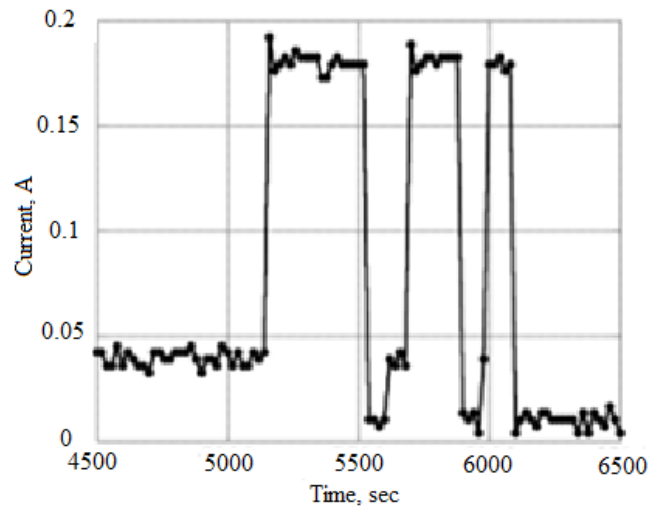


Figure 5. An example of consumption current jump when SEL was observed

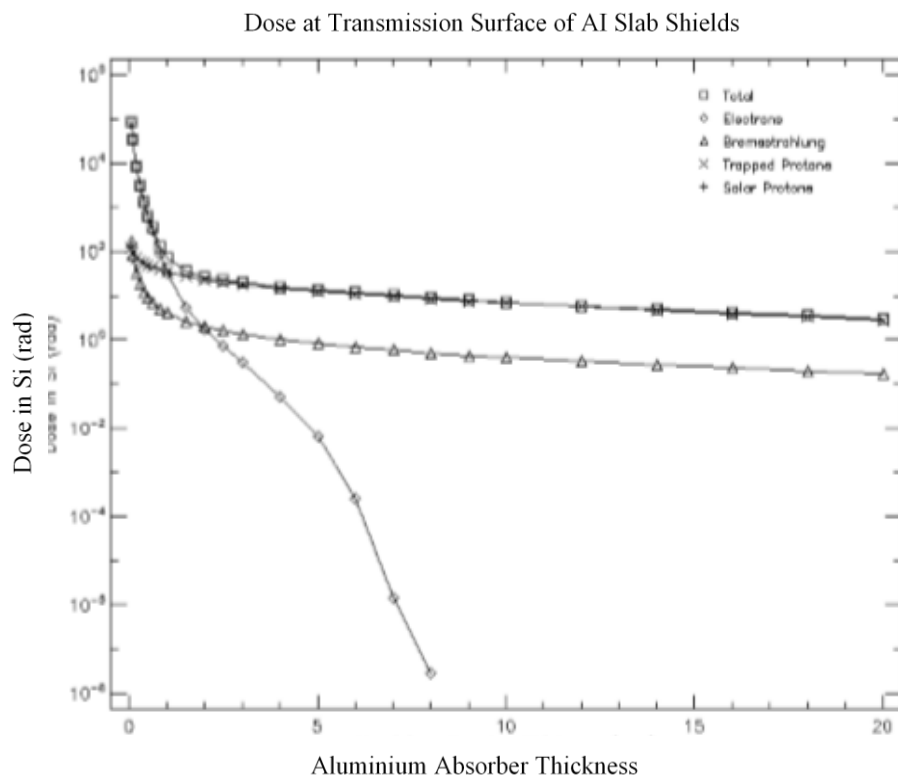


Figure 6. UiTMSAT-1 tested with ionizing dose effect

From the Figure 7 it is clear that the electrons and protons effect start at 10 rad dose and the electron effect was stopped at 8mm of aluminium shielding. The data that tested using ionizing dose effect received from Spenvi only present of the single event upset (SEU). The Figure 7 also shows the SEU effects on UiTMSAT-1. In this Figure the effect of integral flux starts at almost $0.009 \text{ M m}^{-2} \text{ sr}^{-1} \text{ s}^{-1}$ and the effect of differential flux starts at $0.002 \text{ M m}^{-2} \text{ sr}^{-1} \text{ s}^{-1}$. For this also the integral and differential flux is stopped at $5 \times 10^2 \text{ MeV}$ of LET.

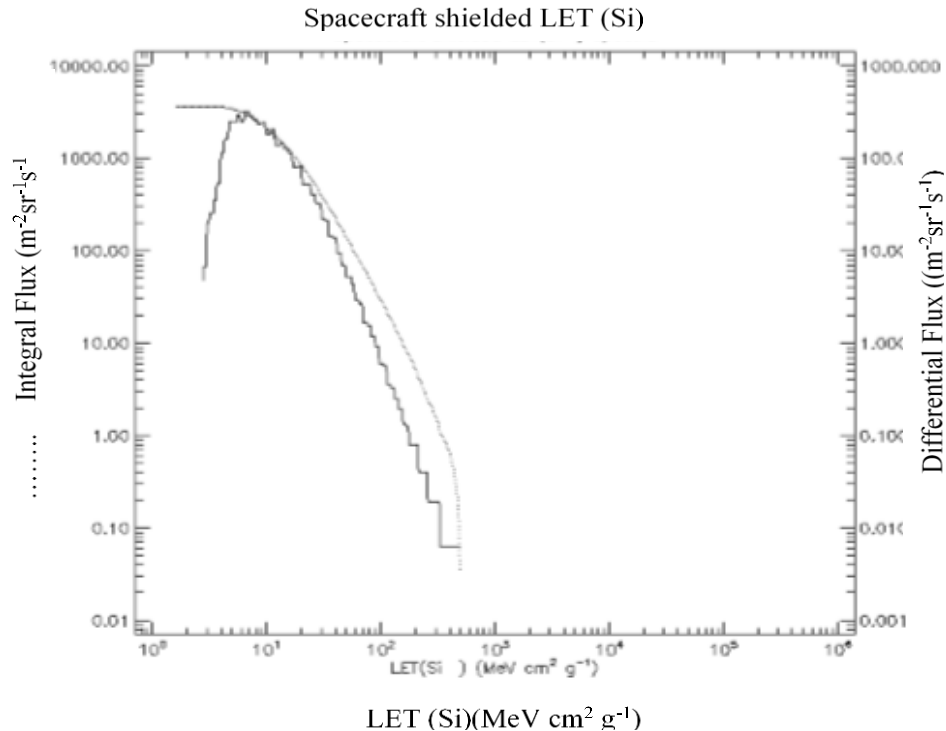


Figure 7. The event effect to UiTMSAT-1

3.3. Mitigate the event

The use of shield to reduce radiation and using software's to analyze the shield thickness and analysis of radiation tolerant circuits is essential. By increasing the thickness of aluminium shielding on satellites, we can reduce the radiation effects. Especially by increasing the shielding size we can reduce TID effects to a minimum because, the electrons causing TID have low penetration capacity. But other radiational effects cannot be stopped by just shielding, to avoid them the electronic components used in the satellites must undergo Radiation Hardening before going to space. Assigning safe orbital path for satellites can also reduce the radiation effects and this is because in the atmosphere at some regions' radiations are extreme.

4. CONCLUSION

This paper presents the SEL detection for nano-satellite external solar radiation mitigation system. The results showed from circuit tested and simulation are different output. Where in the current injection circuit testing was indicate the amount of SEL while in SPENVIS simulation, only SEU effecting was appeared. From this analysis shows both events can harm the OBC and cause the damage to the whole satellite. The mitigation of the SEE must be continuing the researches so that the mission carried can be done and received the desired outcome.

ACKNOWLEDGEMENTS

The authors would like to thank Faculty of Electrical Engineering, Universiti Teknologi MARA (UiTM) for their valuable support. This research is partly funded by the Malaysian Government through UiTM under 600-IRMI/5/3/GIP (0042/2019).

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