

VHDL design and FPGA implementation of direct torque control for induction machines

Elhabib Lotfi, M. Elharoussi, E. Abdelmounim

Department of Applied Physics, ASTI Laboratory, Faculty of Science and Technology (FST) Settat, University Hassan 1st, Settat, Morocco

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ABSTRACT

This paper presents a VHDL design and an FPGA implementation of a direct torque controller (DTC) used to order induction machines (IM). The use of FPGA at high sampling frequency reduces the torque ripple while maintaining the classical DTC control structure. We have adopted a modular approach, by dividing the global entity into a set of elementary blocks designed and implemented separately. The performances of this command are to reduce the torque ripple to 0.01 Nm and the flux ripple to 0.01 wb with a circuit implementing DTC control of 3,256 LEs of complexity and 64 latency clock cycles. To evaluate the performance of our FPGA circuit implementing DTC controller, we have performed a co-simulation platform based on MATLAB/Simulink and Modelsim programs. MATLAB/Simulink was used to simulate the dynamics of the induction machine associated with its inverter and the proposed DTC control strategy was executed under the modelsim software using the VHDL fixed point. We have operated our circuit FPGA in the loop in a speed variation platform of induction machine and we have obtained the following performances: A zero overrun, response time at speeds of 300 ms and a zero static error as required in the specifications.

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Corresponding Author:

Elhabib Lotfi

Hassan 1st University

Faculty of Science and Technology (FST) Settat, Settat, Morocco

Email: lothamid@gmail.com

1. INTRODUCTION

The direct torque controller (DTC) is a technique used in variable speed drives of induction machines to control the electromagnetic torque and the stator flux in a simple and decoupled manner, the original structure of conventional DTC was proposed by Takahashi in 1986 [1], the presence of two hysteresis controllers in the structure of this control induces ripples on the flux and the torque. The evolution of power converter technology and the use of DSP or field-programmable gate array (FPGA) for numerical calculations have allowed the development of complex and robust control algorithms and the development of optimal control techniques for (IM) [2]. The use of a DSP for the implementation of DTC control algorithms with switching frequencies of 20 kHz [3] does not prevent the presence of torque ripples and deterioration of torque and flux estimates, while the use of an FPGA component allows a reduction of the execution time and consequently a high sampling frequency, this paper proposes a design methodology and implementation of the DTC control of an induction machine on an FPGA target with a high sampling frequency.

Very high-speed integrated circuit (VHSIC) hardware description language (VHDL) was used to describe the behavior of the control algorithms. To get simple implementation and fast computation while

minimizing calculation errors and hardware resource usage, we have used a two's complement fixed-point format, a variable word-size approach and a non-restoring method [4] to calculate the square root operation of stator flux. We have begun this work with a general introduction presenting the context of DTC control and the different methods of its digital implementation either on an FPGA target or on a DSP-based target, indicating the contribution of the FPGA implementation compared to DSP techniques, then we will study in section 2 the principle of the DTC command and the mathematical equations of this control strategy. In section 3, we presented and described the design and the proposed implementation for this command block by block, which we will use later to build the FPGA circuit implementing the DTC. In section 4, a Simulink/Modelsim co-simulation platform is given for the validation of the suggested control strategy, the results of the implementation are presented and discussed, a general conclusion and perspectives for this work are presented at the end of this paper.

2. THEORETICAL BASIS OF THE DTC AND THE PROPOSED METHOD

The main objective of the DTC command is to estimate in real-time the values of the torque and the magnetic flux according to the currents and the voltages of the machine. This command imposes on the machine, directly and independently, the torque and the flux by choosing the appropriate voltage vector of the inverter in such a way as to maintain the torque and flux errors within the limits of the hysteresis comparator [5], [6]. Figure 1 shows the principle diagram of the DTC strategy. Both the stator flux and torque controllers are responsible for generating the stator flux and torque error state. The choice of the appropriate voltage vector in the inverter switching table makes it possible to simultaneously control the stator flux and the torque as a function of the current position of the flux and the outputs of the hysteresis comparators.

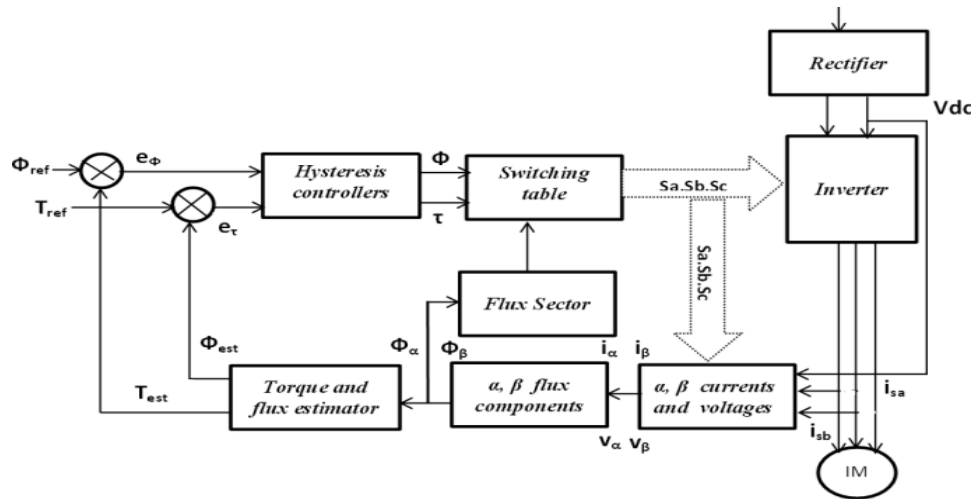


Figure 1. Direct torque control block diagram

2.1. Determination of the α , β currents and voltages signals

This first block of the DTC command projects into a 2-phase reference frame (α , β) the electrical signals of the induction machine expressed in a 3-phase reference frame (a, b, c) by carrying out the transformation of Concordia [7], [8]. The values of the current signals in this new reference frame (i_α , i_β) are obtained from the signals (i_a , i_b) according to (1), (2) while the current state of the switches of the voltage inverter (S_a , S_b , S_c) and the level of the bus V_{dc} make it possible to calculate the values of the voltage signals (v_α , v_β) by respecting (3), (4).

$$i_\alpha = i_a \quad (1)$$

$$i_\beta = \frac{\sqrt{3}}{3} (i_a + 2 i_b) \quad (2)$$

$$V_\alpha = \frac{V_{dc}}{3} (2S_a - S_b - S_c) \quad (3)$$

$$V_\beta = \frac{\sqrt{3}}{3} V_{dc} (S_b - S_c) \quad (4)$$

2.2. The α , β flux components and flux sector detection

The stator flux is calculated based on (5) and (6): [9].

$$\varphi_{\alpha} = \varphi_{\alpha 0} + (V_{\alpha} - R_S i_{\alpha}) T_S \quad (5)$$

$$\varphi_{\beta} = \varphi_{\beta 0} + (V_{\beta} - R_S i_{\beta}) T_S \quad (6)$$

In order to ensure the orientation of the stator flux, we must know its exact position at all times [10], [11], for this, we divide the trajectory of the flux vector ϕ_s into six symmetrical sectors [12], the position of the flux is obtained by calculating the flux angle θ_s based on the α , β flux components [13] as indicated in the (7):

$$\theta_s = \tan^{-1} \frac{\varphi_{\beta}}{\varphi_{\alpha}} \quad (7)$$

2.3. Torque and flux estimator

The stator magnetic flux and the electromagnetic torque are expressed by the (8) and (9): [14], [15]:

$$\varphi_s = \sqrt{\varphi_{\alpha}^2 + \varphi_{\beta}^2} \quad (8)$$

$$T_e = \frac{3}{2} p (\varphi_{\alpha} i_{\beta} - \varphi_{\beta} i_{\alpha}) \quad (9)$$

2.4. Hysteresis controllers

The hysteresis controllers allow us to provide the flux and torque error state according to the difference between the reference values and the estimated values. We have chosen to use, as shown in Figure 2, a 2-level hysteresis controller for the flux and a 3-level hysteresis controller for the torque [16], [17].

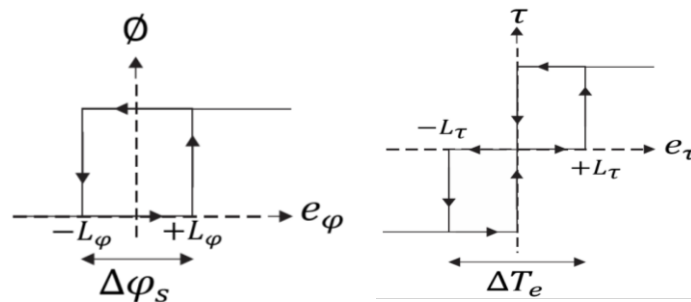


Figure 2. Hysteresis controllers

2.5. Switching table

This block generates the appropriate voltage vector (S_a , S_b , S_c), among the six possible active vectors (V_1 - V_6) or the two null vectors (V_0 , V_7), from the inverter optimal switching table [18], presented in Table 1, depending on the current position of the stator flux (expressed by sector) and the flux and torque error state ϕ , τ the outputs of the hysteresis comparator [19].

Table 1. Optimum switching table

		Sector					
ϕ	τ	1	2	3	4	5	6
1	1	$V_2(110)$	$V_3(010)$	$V_4(011)$	$V_5(001)$	$V_6(101)$	$V_1(100)$
	0	$V_7(111)$	$V_0(000)$	$V_7(111)$	$V_0(000)$	$V_7(111)$	$V_0(000)$
	-1	$V_6(101)$	$V_1(100)$	$V_2(110)$	$V_3(010)$	$V_4(011)$	$V_5(001)$
0	1	$V_3(010)$	$V_4(011)$	$V_5(001)$	$V_6(101)$	$V_1(100)$	$V_2(110)$
	0	$V_0(000)$	$V_7(111)$	$V_0(000)$	$V_7(111)$	$V_0(000)$	$V_7(111)$
	-1	$V_5(001)$	$V_6(101)$	$V_1(100)$	$V_2(110)$	$V_3(010)$	$V_4(011)$

3. PROPOSED DESIGN METHOD

The DTC algorithm was designed on the basis of a structural description by adopting the concept of modularity and reusability of the various VHDL blocks of the architecture. We opted during the VHDL design for the use of a two's complement fixed-point format and variable word size for all arithmetic calculations. The data size of our system starts with 12 bits and increases with mathematical operations to keep good precision without consuming too much hardware resources. Our architecture is composed of seven main parts Figure 3, designed and implemented separately, placing all the blocks inside high-level design using component instantiation, and connecting up all the components to each other using port mapping. the syncpulse block (block A) in charge of the control of all the other DTC blocks in order to have a constant sampling period (T_s), the α , β currents and voltages signals (block B), the α , β flux components (block C), the torque and flux estimator (block D), the Hysteresis controllers (block E), the flux sector detection (block F) and the switching table (block G) which generates the pulses to be applied to the various arms of the inverter. We have adopted a modular approach [20]-[22] to realize our architecture, we will propose, study and validate each module of our design using the FPGA CYCLONE II of Altera EP2C35F672C6 for the implementation and Quartus II software for the compilation and simulation of the different VHDL models. Figure 4 shows the DTC RTL scheme.

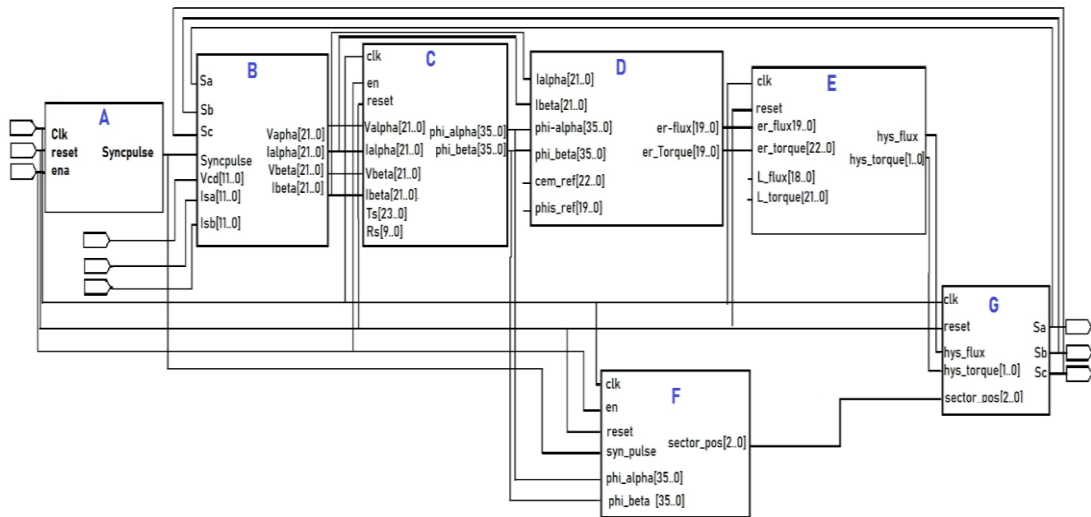


Figure 3. DTC blocks

3.1. Determination of the α , β currents and voltages signals

This block projects into a 2-phase reference frame (α , β) the electrical signals of the induction machine expressed in a 3-phase reference frame (a, b, c). The values of the current signals in this reference frame (i_α , i_β) are obtained from the signals (i_{sa} , i_{sb}) while the current state of the switches (S_a , S_b , S_c) and the level of the bus V_{cd} make it possible to calculate the values of the voltage signals (v_α , v_β) the structure of this block is illustrated in Figure 5. Figure 6 shows the functional simulation of the α , β currents and voltages signals. Currents and voltages signals obtained by this block correspond to the theoretical values given by the Concordia transformation.

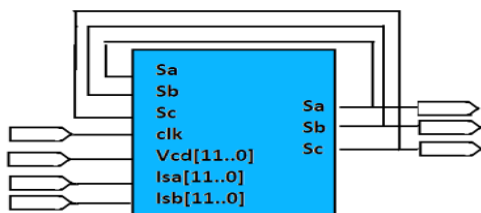


Figure 4. DTC RTL scheme

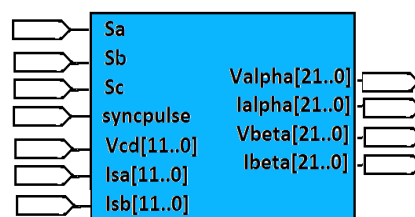


Figure 5. VHDL model of the α , β currents and voltages signals

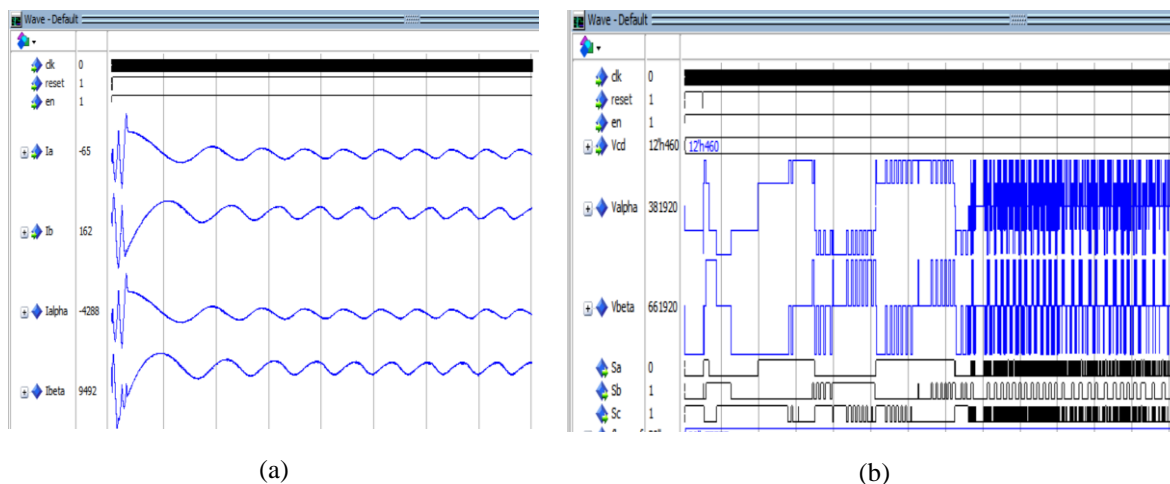


Figure 6. Functional simulation of the α , β currents and voltages signals, (a) α , β currents signals, (b) α , β voltages signals

3.2. α , β flux components

The determination of the flux components φ_{α} and φ_{β} is based on (5) and (6), this calculation is carried out in the same way from the signals of currents and voltages α , β . Therefore, only one block has been designed for this calculation and is used twice in parallel. The VHDL model of the α , β flux components is illustrated in Figure 7. Figure 8 shows the functional simulation of the α , β flux components. The flux components evolve in a sinusoidal manner and have maximum amplitude equal to the setpoint.

3.3. Flux sector detection

Classical techniques use the CORDIC algorithm to determine the sector of the flux vector [23]. In our architecture we used a simpler method, without any angle calculation, based on simple combinatorial [24] by exploiting the data provided by Table 2 to analyze the flux sectors so as to obtain a more reduced calculation time and low complexity. The VHDL model and the functional simulation of this block are given in Figure 9.

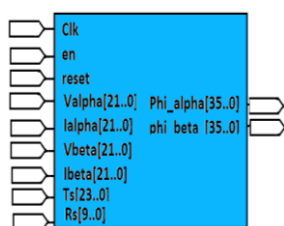


Figure 7. VHDL model of the α , β flux components

Table 2. Flux sector detection

sector	sign φ_{α} & sign φ_{β}	$ \varphi_{\alpha} > \sqrt{3} \varphi_{\beta} $
1	01	1
1	00	1
2	00	0
3	10	0
4	10	1
4	11	1
5	11	0
6	01	0

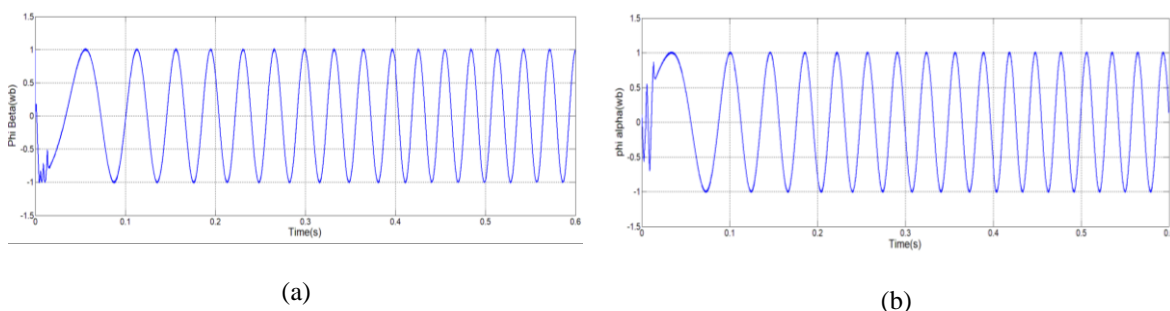


Figure 8. Functional simulation of the, (a) α flux components, (b) β flux components

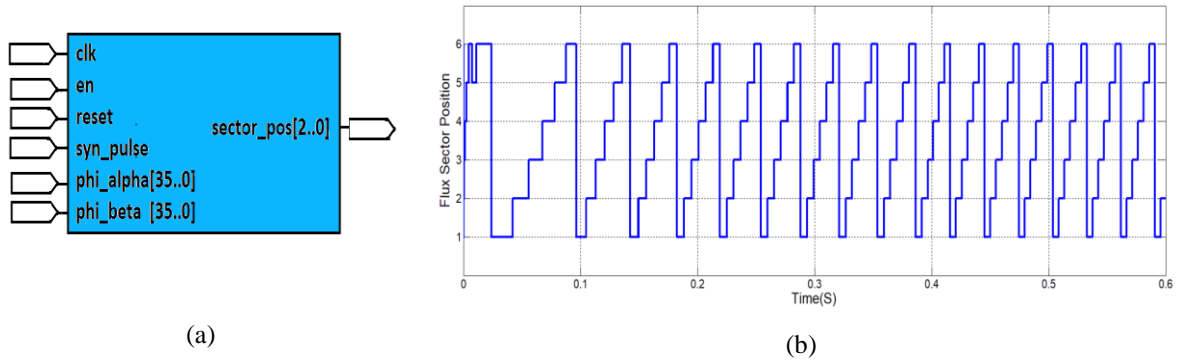


Figure 9. VHDL model and functional simulation of the flux sector detection, (a) VHDL model, (b) Functional simulation

3.4. The torque and flux estimator

This block calculates both the amplitude of the flux from (8) and the torque using (9). The non-restoring method is used to calculate the square root in the expression of the flux, a special architecture has been designed for the squareroot (SQRT). In parallel with this calculation a subtractor generates the difference between the estimated values of flux and torque and the corresponding reference values. The structure of this block is shown in Figure 10. The functional simulation of the torque and flux estimator are given in Figure 11. We notice that the torque and the flux are constant and follow the set point after a very fast transient regime, moreover, the system works with a reduced sampling period, which has allowed us to reduce the torque ripple to 0.01 Nm and the flux ripple to 0.01 Wb as indicated in the results.

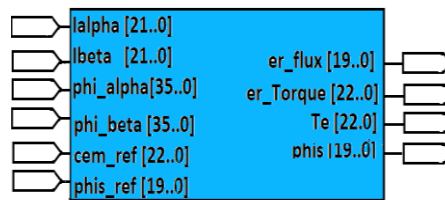


Figure 10. VHDL model of the torque and flux estimator

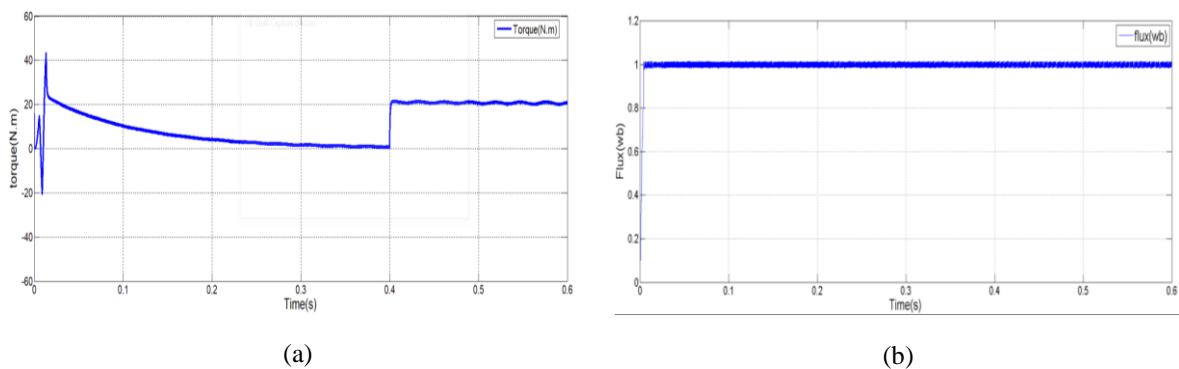


Figure 11. Functional simulation of the torque and flux estimator, (a) Torque, (b) Flux

3.5. The hysteresis comparators

The function of this block is to generate the appropriate error status of the stator flux and torque. The use of 2 and 3 level hysteresis controllers require the representation of their outputs respectively on 1 and 2 bits. The VHDL model and the functional simulation of Hysteresis comparators are given in Figure 12.

3.6. The switching table

The appropriate voltage vector (S_a , S_b , S_c) is selected based on the flux and torque error state (hys_torque , hys_flux) from the inverter optimal switching table and depending on the current position of the stator flux ($sector_pos$). The VHDL model and the functional simulation of the switching table are shown in Figure 13.

3.7. The syncpulse block

This block is responsible for controlling all the other DTC blocks, in order to have a constant sampling period and therefore avoid the major drawback of conventional DTC which is known by unpredictable inverter switching frequency. The architecture and the functional simulation for the syncpulse block are shown in Figure 14. The choice of the sampling period must take into account the maximum frequency of the inverter, the latency of the control circuit and the dynamics of the process to be controlled, for our case of study a period of $5\ \mu s$ satisfying all its constraints.

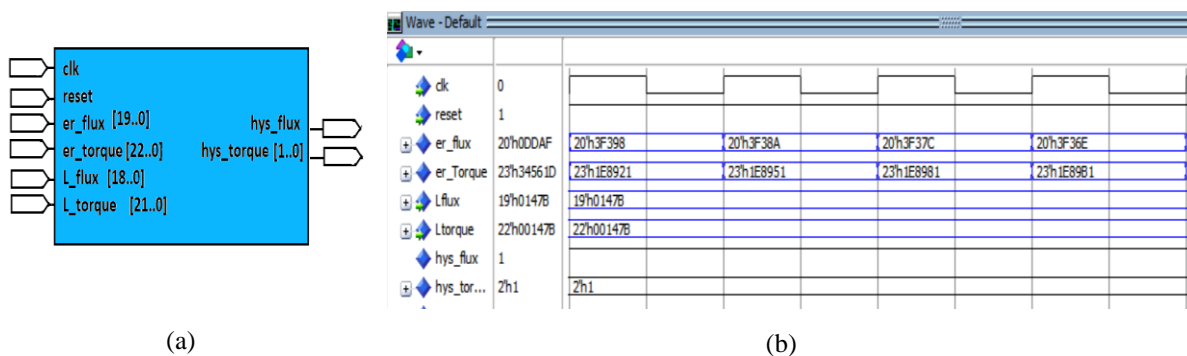


Figure 12. VHDL model and functional simulation of the hysteresis comparators, (a) VHDL model, (b) Functional simulation

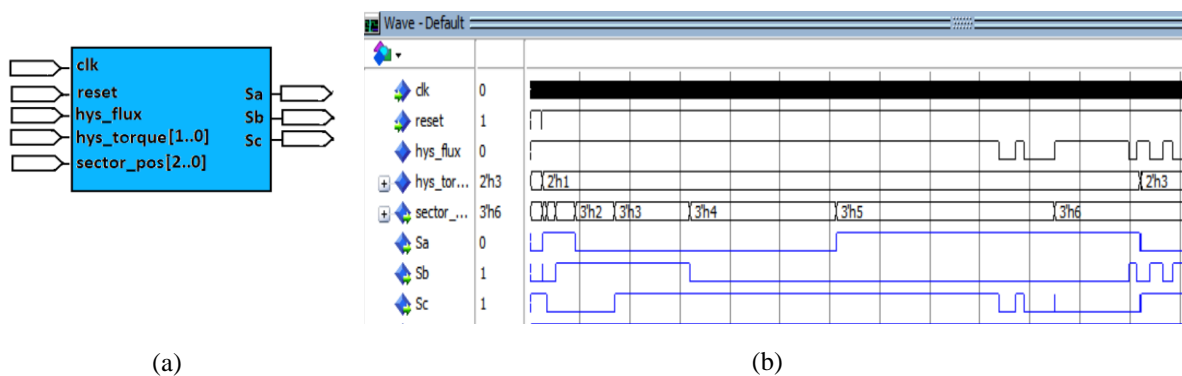


Figure 13. VHDL model and functional simulation of the switching table, (a) VHDL model, (b) Functional simulation

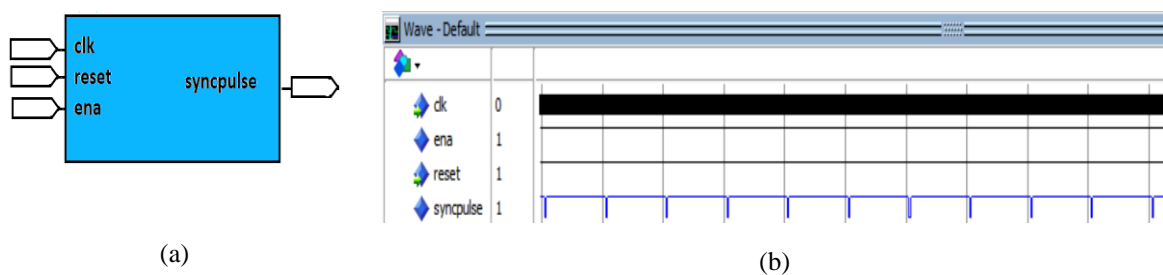


Figure 14. VHDL model, (a) Functional simulation, (b) Of the syncpulse block

4. RESULTS AND DISCUSSION

4.1. Simulink/modelsim co-simulation platform

To validate the proposed FPGA circuit implementing DTC control, a co-simulation was realized with MATLAB/Simulink and Modelsim programs. The MATLAB/Simulink was used to simulate the model of the induction machine associated with the inverter and the VHDL program proposed for the DTC command was executed under Modelsim. Table 3 shows the machine parameters used for simulation. We have operated our circuit in a speed variation platform of induction machines (a resistant torque of 20 N.m is applied to the machine at the instant $t=0,4$ s), and we have fixed the following performances: A zero overrun, a response time in speeds of 300 ms and a zero static error. In this section we will, first of all, validate the DTC command under MATLAB/Simulink, then we will place our circuit FPGA in the loop in the proposed Simulink/Modelsime co-simulation platform.

4.2. Validation of the DTC architecture under MATLAB/Simulink

The simulation of the DTC control established under MATLAB/Simulink has allowed us to validate both the model of the machine and its inverter and also to show the strengths and weaknesses of this command and compare them with those obtained with the command based on the FPGA. Figure 15 shows the architecture of DTC under MATLAB/Simulink. Figures 16 and 17 show the results of the DTC control under MATLAB/Simulink. This command allows a decoupled control of the torque and the flux of the induction machine as illustrated in Figures 16 and 17 but we note that the torque and flux ripples are according to the width of the controller's band and therefore the reduction of this band allows the decrease of the ripples but at the expense of the increase in switching losses.

Table 3. Machine parameters

Elements	Value
Power	3 KW
R_s	0.85Ω
R_r	0.16Ω
L_s	0.16 H
L_r	0.023 H
M_{sr}	0.058 H
J	0.05 kg.m ²
f	0.005 N.m/rad. s ⁻¹
T_s	0.188 s
T_r	0.144 s

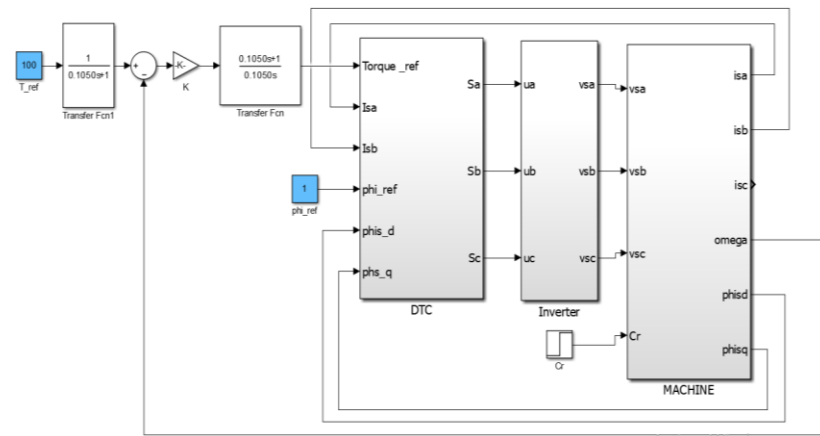


Figure 15. DTC MATLAB/Simulink model

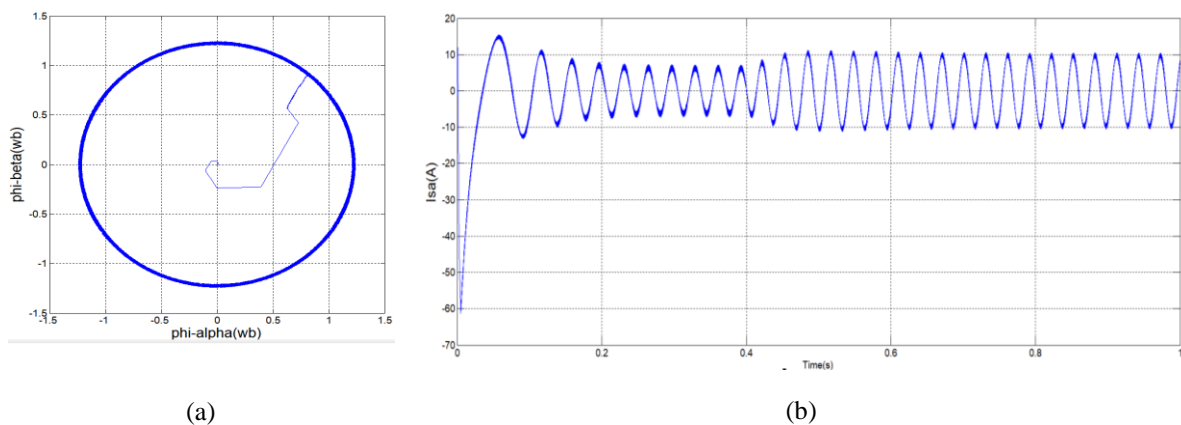


Figure 16. Simulation results, (a) Root locus of the flux, (b) Line current evolution

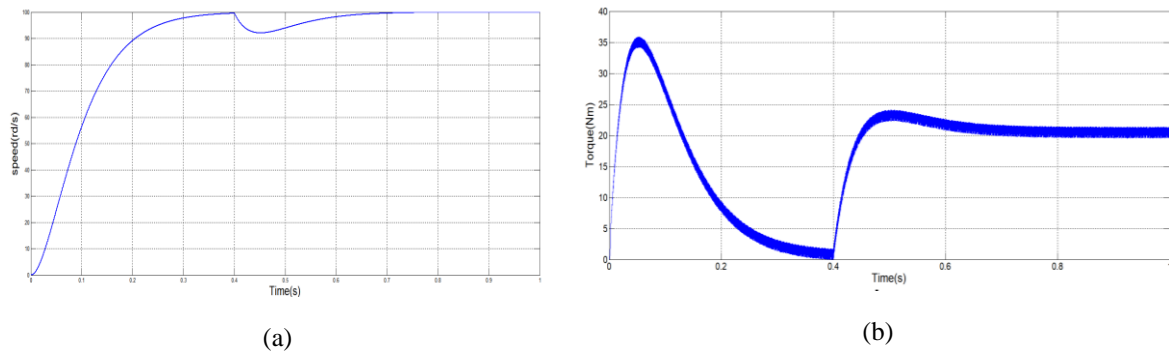


Figure 17. Simulation results, (a) Speed, (b) Torque evolution

4.3. Validation of the DTC-FPGA in the loop

Figure 18 shows the architecture of the MATLAB/Simulink co-simulation of an asynchronous machine modeled under MATLAB/Simulink associated with an inverter and the proposed FPGA circuit implementing DTC control in the loop. Figures 19-21 show the results of the DTC in the loop. The results obtained, as shown in the Figures 19-21 show the reduction of the ripples on the couple as well as the evolution of the flux in the form of a circle with weak undulations, this thanks to the use of a sampling period fixed ($5 \mu\text{s}$) and the reduction of the bandwidth of the hysteresis controllers to 0.01 Nm for the torque and 0.01 Wb for the flux, we also note that the current signals I_{sa} and I_{sb} appear as sinusoidal. Figure 21 shows the evolution of the speed. we note that this command allows a zero overshoot, a response time at speeds of 300 ms and a zero-static error with respect to the setpoint and the disturbance.

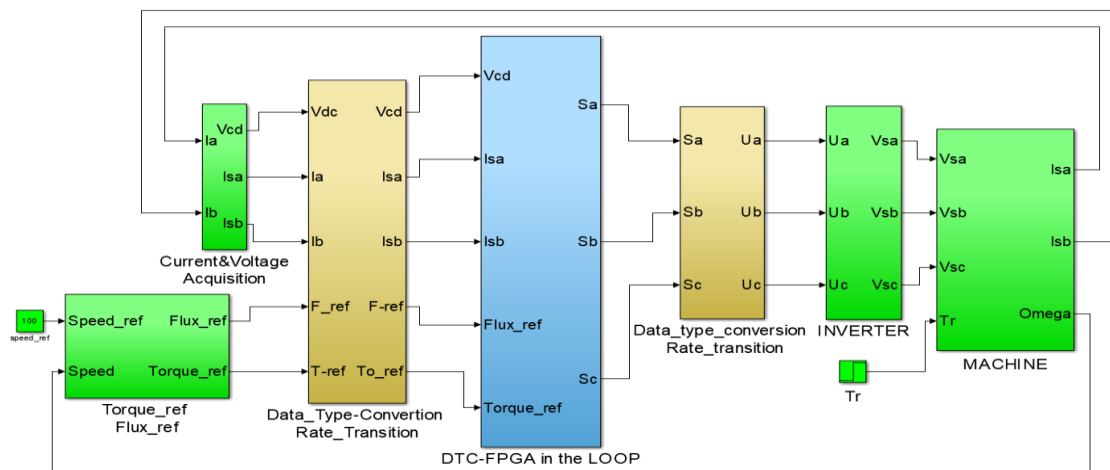
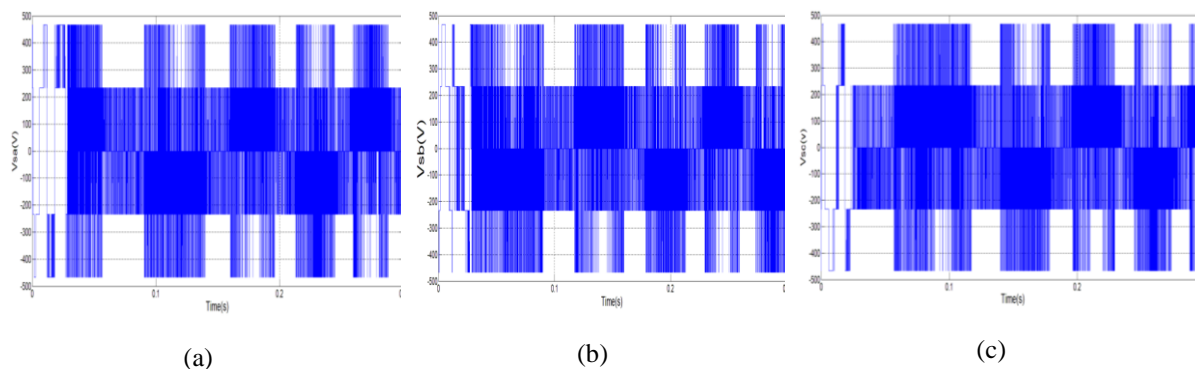


Figure 18. DTC in the loop

Figure 19. Voltages signals, (a) V_{sa} , (b) V_{sb} , (c) V_{sc}

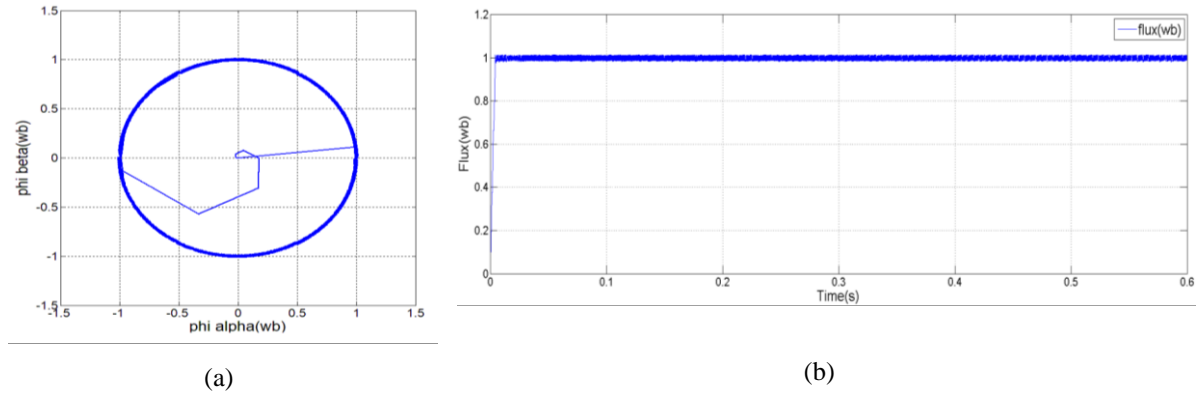


Figure 20. Flux evolution, (a) Root locus of the flux, (b) Flux vs time

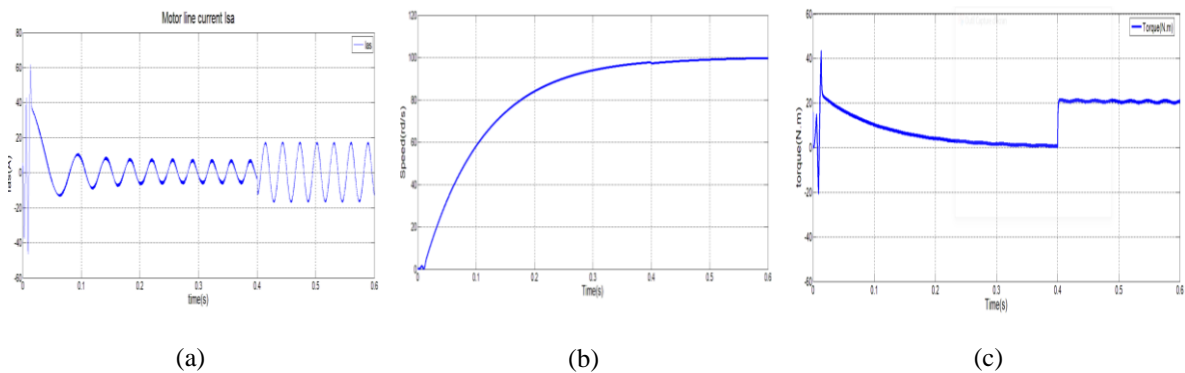


Figure 21. Evolution, (a) Current, (b) Speed, (c) Torque evolution

4.4. Performance analysis and effect of the sampling time to torque ripple

The major drawback of conventional DTC is the unpredictable switching frequency of the inverter. Therefore, the amplitude of the hysteresis band must be large enough to avoid excessive switching which causes relatively large torque ripples; our circuit operates with a constant switching frequency. The use of the FPGA target to implement the DTC allowed us to minimize and fix the sampling period. Table 4 represents the FPGA resources available and those consumed by our circuit. The experiment was conducted on CYCLONE II of Altera type EP2C35F672C6 and consumes 3,256 logic elements for the implementation. We have increased the frequency in such a way as to reduce the ripple torque while keeping the same level of complexity as the works [8], [10], [25], [26].

Table 4. The resources available and those consumed by our architecture

Elements	Available	used	Percentage
Logic Registers	33216	1,244	< 1 %
Total Logic Elements	33216	3,256	10%
Total Pins	475	278	59 %
Total Combinational Functions	33216	2,549	7.6%
Embedded Multiplier 9-bit Elements	70	57	81%
Total PLLs	4	0	0 %
Total DLLs	2	0	0 %

5. CONCLUSION

In this paper, we have developed and implemented on FPGA a DTC control strategy of an induction motor. The DTC was preferred to other control techniques thanks to its simplicity and its high performance in motor control. Although DTC presents a large ripple on flux and torque signals, it was possible to minimize it to a low value by reducing the sampling period, this reduction was achieved by using FPGA implementation of the DTC algorithm thanks to parallel processing techniques and VHDL programming aimed at reducing the latency of the circuit when approaching a system real-time by the application of a simple architecture for

the different blocks of the DTC command and in particular in the torque/flux estimator. We have proposed an FPGA circuit implementing DTC control and we have realized a platform based on MATLAB / Simulink and Modelsim co-simulation of the speed variation of an asynchronous machine. The results obtained enabled us to validate our DTC-FPGA circuit. Comparatively to the conventional DTC controller the proposed architecture has a slight advantage. The obtained performances from this command are 3,256 LEs of complexity and 64 latency clock cycles with the torque ripple equal to 0.01Nm and the flux ripple is 0.01wb. As a forthcoming application, the DTC-SVM control of an induction machine should be performed while exploiting the DTC-FPGA circuit and the co-simulation platform proposed in this paper.

REFERENCES

- [1] I. Takahashi and T. Noguchi, "A New Quick-Response and High-Efficiency Control Strategy of an Induction Motor," in *IEEE Transactions on Industry Applications*, vol. IA-22, no. 5, pp. 820-827, Sept. 1986, doi: 10.1109/TIA.1986.4504799.
- [2] E. Lotfi, B. Rached, M. Elharoussi, and E. Abdelmounim, "DSP Implementation in the Loop of the Vector Control Drive of a Permanent Magnet Synchronous Machine," *ACM International Conference Proceeding Series (ICPS)* no. 53, pp. 1-7, November 2017, doi: 10.1145/3167486.3167542.
- [3] S. M. A. Cruz, H. A. Toliyat, and A. J. M. Cardoso, "DSP implementation of the multiple reference frames theory for the diagnosis of stator faults in a DTC induction motor drive," in *IEEE Transactions on Energy Conversion*, vol. 20, no. 2, pp. 329-335, June 2005, doi: 10.1109/TEC.2005.845531.
- [4] S. Samavi, A. R. Sadrabadi, and A. Fanian, "Modular array structure for non-restoring square root circuit," *Journal of Systems Architecture*, vol. 54, pp. 957-966, October 2008, doi: 10.1016/j.sysarc.2008.04.004.
- [5] T. Sutikno, N. R. N. Idris, and A. Z. Jidin, "A Model of FPGA-based Direct Torque Controller," *TELKOMNIKA Telecommunication, Computing, Electronics and Control*, vol.11, no. 2, pp. 747-753, February 2013, DOI: 10.11591/telkomnika.v11i2.2002.
- [6] T. Sutikno, N. R. N. Idris, and A. Jidin, "A Review of Direct Torque Control for Induction Motors for Sustainable Reliability and Energy Efficient Drives," *Renewable and Sustainable Energy Reviews (RSER)*, vol. 32, pp. 548-558, 2014, doi: 10.1016/j.rser.2014.01.040.
- [7] A. Jidin, N. R. N. Idris, A. H. M. Yatim, T. Sutikno, and M. E. Elbuluk, "An Optimized Switching Strategy for Quick Dynamic Torque Control in DTC-Hysteresis-Based Induction Machines," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3391-3400, Aug. 2011, doi: 10.1109/TIE.2010.2087299.
- [8] A. Llor, B. Allard, X. Lin-Shi, and J-Retif, "Comparison of DTC implementations for synchronous machines," *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, Aachen, Germany, 2004, pp. 3581-3587 Vol.5, doi: 10.1109/PESC.2004.1355109.
- [9] T. Sutikno, N. R. N. Idris, A. Jidin, and M. N. Cirstea, "An Improved FPGA Implementation of Direct Torque Control for Induction Machines," in *IEEE Transactions on Industrial Informatics*, vol. 9, no. 3, pp. 1280-1290, Aug. 2013, doi: 10.1109/TII.2012.2222420.
- [10] R. Rajendran and N. Devarajan, "Simulation and Implementation of a High-Performance Torque Control Scheme of IM Utilizing FPGA," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 2, no. 3, pp. 277-284, June 2012, doi: 10.11591/ijece.v2i3.208.
- [11] D. D. Casadei, G. Serra, and K. Tani, "Implementation of a direct control algorithm for induction motors based on discrete space vector modulation," in *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 769-777, July 2000, doi: 10.1109/63.849048.
- [12] E. Lotfi, M. Elharoussi, and E. Abdelmounim, "VHDL Design and FPGA Implementation of the SVPWM of a Three-phase Asynchronous Machine Powered by a Voltage Inverter," *International Review on Modeling and Simulations (IREMOS)*, vol. 10, no. 4, pp. 232-238, August 2017, doi: 10.15866/iree.v14i1.13928.
- [13] N. El-Ouanjli, A. Derouich, and A. El Ghzizal, "Modern improvement techniques of direct Torque control for induction motor drives-a review," *Protection and Control of Modern Power Systems*, vol. 4, no. 1, pp. 1-12, 2019, doi: 10.1186/s41601-019-0125-5.
- [14] E. Monmasson and M. N. Cirstea, "FPGA Design Methodology for Industrial Control Systems-A Review," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 1824-1842, Aug. 2007, doi: 10.1109/TIE.2007.898281.
- [15] K.S. Gdaim, S. Mtibaa, and A. F. Mimouni, "FPGA-Based Implementation Direct Torque Control of Induction Motor," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 5, no. 3, pp. 293-304, February 2015, doi: 10.11591/ijpeds.v5.i3.pp293-304.
- [16] B. Hariram and N. S. Marimuthu, "FPGA Based Speed Control of Induction Motor," *International Journal on Engineering Applications (IREA)*, vol. 4, no. 6, pp. 194-200, 2016.
- [17] I. Bahri, L. Idkhajine, E. Monmasson, and M. El Amine Benkhelifa, "Hardware/Software Codesign Guidelines for System on Chip FPGA-Based Sensorless AC Drive Applications," in *IEEE Transactions on Industrial Informatics*, vol. 9, no. 4, pp. 2165-2176, Nov. 2013, doi: 10.1109/TII.2013.2245908.
- [18] J. Lis, C. T. Kowalski, and T. Orłowska-Kowalska, "Sensorless DTC control of the induction motor using FPGA," *2008 IEEE International Symposium on Industrial Electronics*, Cambridge, UK, 2008, pp. 1914-1919, doi: 10.1109/ISIE.2008.4677287.

- [19] B. Bossoufi, M. Karim, A. Lagrioui, and G. Iana, "Comparison Of The Fpga-Based Implementation And MATLAB/Simulink Simulation Torque Controller Of A PMSM Machine Drive," *International Science and Technology Conference* 7-9 Istanbul, December 2011.
- [20] B. Bossoufi, M. Karim, I. Silviu and A. Lagrioui, "FPGA-based implementation by direct torque control of a PMSM machine," *2011 7th International Conference-Workshop Compatibility and Power Electronics (CPE)*, Tallinn, Estonia, 2011, pp. 464-469, doi: 10.1109/CPE.2011.5942251.
- [21] M. Habibullah, D. D. Lu, D. Xiao, and M. F. Rahman, "A Simplified Finite-State Predictive Direct Torque Control for Induction Motor Drive," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3964-3975, June 2016, doi: 10.1109/TIE.2016.2519327.
- [22] O. Sandre-Hernandez, J. J. Rangel-Magdaleno, and R. Morales-Caporal, "Simulink-HDL cosimulation of direct torque control of a PM synchronous machine based FPGA," *2014 11th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)*, Ciudad del Carmen, Mexico, 2014, pp. 1-6, doi: 10.1109/ICEEE.2014.6978298.
- [23] M. A. Zare, R. G. Kavasseri, and C. Ababei, "FPGA-based design and implementation of direct torque control for induction machines," *2014 International Conference on ReConFigurable Computing and FPGAs (ReConFig14)*, Cancun, Mexico, 2014, pp. 1-6, doi: 10.1109/ReConFig.2014.7032520.
- [24] E. Lotfi, M. Elharoussi, and E. Abdelmounim, "VHDL Design and FPGA Implementation of the PWM Space Vector of an AC Machine Powered by a Voltage Inverter," *Lecture Notes in Electrical Engineering*, vol 381, Springer, Cham. 2016, doi: 10.1007/978-3-319-30298-0_5.
- [25] Y. Utsumi, N. Hoshi, and K. Oguchi, "Comparison of FPGA-based Direct Torque Controllers for Permanent Magnet Synchronous Motors," *Journal of Power Electronics*, vol. 6, no. 2, pp. 114-120, 2006
- [26] S. Boukadida, S. Gdaim, and A. Mtibaa, "A Novel Direct Torque Control for Induction Machine Drive System with Low Torque and Flux Ripples using XSG," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 4, no. 4, pp. 517-527, December 2014.

BIOGRAPHIES OF AUTHORS



Elhabib Lotfi is graduated from the High Normal School of Technical Education (ENSET) in 1998 at RABAT Morocco. In 2007, he had the diploma of aggregation in electrical engineering at ENSET of Rabat Morocco. In 2014 he obtained the Master in Automatic, Signal Processing and Industrial Computer Science from the Faculty of Science and Technology (FST), Hassan I University, Settat Morocco. Currently, he is a PhD student at the System Analysis and Information Technology Laboratory at Hassan I University, Settat, Morocco.



Mustapha Elharoussi received his Ph. D in Error Correcting Codes from Mohammed V University Morocco in 2013. In 2014 he joined, as Professor, applied Physics department of FST, Hassan I University, Settat, Morocco. His current research interests include hardware design of algorithms applied to information processing and control of industrial systems at System Analysis and Information Technology Laboratory at Hassan I University, Settat, Morocco.



Elhassane Abdelmounim received his PhD in Spectral analysis from Limoges University France in 1994. In 1996, he joined, as Professor, applied physics department of FST, Hassan I University, Settat, Morocco. His current research interests include digital signal processing and machine learning. He is currently the coordinator of a Bachelor of Science in electrical engineering and he is researcher at System Analysis and Information Technology Laboratory at Hassan I University, Settat, Morocco.