High gain over an octave bandwidth class-F RF power amplifier design using 10W GaN HEM

Noor Syakirah Ruslan Hadi¹, Zubaida Yusoff², Md. Golam Sadeque³, Shaiful Jahari Hashim⁴, Muhammad Akmal Chaudhary⁵

^{1,2,3}Faculty of Engineering, Multimedia University, Malaysia
⁴Faculty of Engineering, University Putra Malaysia, Malaysia
⁵Department of Electrical Engineering, Ajman University, UAE

Article Info

Article history:

Received Nov 30, 2019 Revised Mar 8, 2020 Accepted Apr 9, 2020

Keywords:

Class-F GaN HEMT Power added efficiency RF power amplifier Wideband

ABSTRACT

The wireless communication industry grows faster each day. In terms of RF power amplifier (RFPA), the requirements on efficiency, linearity, bandwidth, output power and cost are getting more stringent. RFPA is considered as the most important component because of consuming large power in a base station. In this paper, a systematic approach is used to design a high flat gain class-F RFPA over an octave bandwidth. The simulation of a 1.5GHz class-F power amplifier mode demonstrates a high drain efficiency while accomplishing a high flat gain over a wide bandwidth. To identify the optimum impedance for the output matching and input matching network, the load-pull and source-pull are performed. The simulation results show that the RFPA can deliver a drain efficiency of 68.37 % at the output power of 40.79 dBm with power added efficiency of 66.94 %. The designed PA achieved a high gain between 13 dB to 17 dB from 0.5 GHz to 2.0 GHz of a frequency band. The matching circuits are realized on an FR-4 substrate to keep the cost as low as possible. A 10W GaN HEMT CGH40010 transistor from Cree has been used for this RFPA design.

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Corresponding Author:

Zubaida Yusoff, Faculty of Engineering, Multimedia University,

Jalan Multimedia, 63100 Cyberjaya, Selangor, Malaysia.

Email: zubaida@mmu.edu.mv

1. INTRODUCTION

The development for incoming 5G communications in wireless technologies has led to an increased demand for wide bandwidth, high efficiency and lower operational cost of radio frequency power amplifier (RFPA). These criteria are crucial as the 5G network enables higher data rate, higher system capacity, and low latency, therefore it can support a wider range of services compared to previous technologies [1]. In addition, important features such as wide bandwidth, high efficiency and a moderate power RFPA in a microcell network able to provide radio coverage to a smaller area of mobile network access which increases the network capacity. Wideband RFPA design is popular because it can allow operation at various frequency bands. Also, a wideband RFPA will realize better real-time communication and fasten the data rate. A higher efficiency power amplifier is also important to decrease the level of DC power consumption [2] which also results in a lower cooling requirement and at the same time decreasing the operating cost of the system [3].

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Class-F has gained importance compared to other amplifier classes since it can produce both high output power and power-added efficiency due to its switching characteristics. Theoretically, the class-F amplifier able to achieve up to 100% efficiency with harmonic resonators being implemented at the output network in order to shape the drain and collector waveforms [4]. The load appears to be short at even harmonic and an open circuit at odd harmonic. The drain current waveform takes one or more even harmonics to achieve a half-wave rectified sinusoidal whereas the drain voltage waveform takes a few odd harmonics to achieve a square wave [5, 6].

Transistor selection is highly important in implementing a high power amplifier. In recent years, GaN technology is chosen for developing the wideband RFPA because GaN is a wide bandgap material that offers high breakdown voltage, high-temperature applications and higher carrier mobility [7]. The high power density property of GaN results in the reduction of the parasitic capacitance. This reduced parasitic capacitance improves the bandwidth of the RFPA when designing for the impedance matching, as compared to other technologies [8]. A GaN HEMT is also chosen because of its high thermal conductivity so it is more reliable for high power operation. It is found that the device can operate up to 6 GHz and is able to deliver a maximum output power of 40 dBm when referred to the datasheet of Cree CGH40010.

There are several wideband and high-efficiency class-F power amplifiers have been designed and simulated in the literature using 10 W Cree GaN HEMT CGH40010. A broadband PA biased in class-F mode with a drain current of 163 mA is presented in [9]. The design is based on harmonic control technique and achieves drain efficiency of 55-66 % and power added efficiency (PAE) higher than 50%, along with 40-42dBm output power for a coverage band of 1.6-3.8 GHz. A flat gain of 8-10 dB is obtained. The impedances obtained from load-pull test bench in Agilent ADS are realized in matching networks with passive components, microstrip lines and open circuit stubs. The design is printed on an FR-4 substrate. A highly efficient broadband class-F power amplifier with multiples of harmonic controlled at the output network is presented in [10]. The design achieved a gain of 10-15 dB, a maximum output power of 40 dBm and a saturated drain efficiency of 60% to 73% throughout the selected frequency band from 1.1 to 2.1 GHz. A multi-stage low-pass output matching network is also designed and implemented in microstrip technology to efficiently deal with the parasitic of the packaged device. The complete RFPA is fabricated on an FR-4 substrate. Another design [11] is concerned with a wide bandwidth from 0.5 to 2.3 GHz. Over this frequency range, drain efficiency obtained is more than 60% with output power greater than 39 dBm and a larger signal gain of more than 11.7 dBm. The conventional continuous class-F RFPA is extended in order to maintain high efficiency over a wide bandwidth, which can be used to simplify the design procedure for the second harmonic and also fundamental frequencies. The circuit is fabricated using the Rogers substrate RO4003C.

In this work, a high flat gain over an octave bandwidth class-F power amplifier with frequency band from 0.5 to 2.0 GHz centered at 1.5 GHz is designed and simulated using a 10W CGH40010 GaN HEMT. 1.5 GHz is categorized in L band frequency range and it is the operating ranges used by applications like radars, radio, telecommunications, a global positioning system (GPS) and aircraft surveillance [10, 12]. Load and source-pull simulations are applied to the frequencies up to third-order harmonic in order to achieve an optimum half-wave rectified sinusoidal at drain current while at the drain voltage, a square waveform is achieved. The parasitic de-embedding network is also applied to present the right output waveforms at the current-generator plane. The maximum PAE and drain efficiency achieved are 66.94 % and 68.37% at the output power of 40.79 dBm. Among all the work in the state-of-art table as shown in Table 1, the highest flat gain of 13-17 dB for the entire band is achieved in this work. The overall performance of the designed RFPA in this paper is compared with other works in the state-of-art Table 1 of 10W (CGH40010) GaN HEMT based wideband class-F power amplifiers.

Table 1. State-of art wideband class-F RFPA

Reference	Bandwidth (GHz)	Gain (dB)	Drain Efficiency (%)	Pout (dBm)
2014 [5]	1.6-3.8	8-10	55-66	42
2016 [6]	1.1-2.1	10-15	73	40
2018 [7]	0.5-2.3	>11.7	>60	>39
This work	0.5-2.0	13-17	68.37	40.79

2. RESEARCH METHOD

Class-F RFPA is designed according to the design process as shown in Figure 1. The circuit design and simulations are carried out using Keysight ADS (advanced design system) CAD software. The circuit design for class-F power amplifier begins with the selection of a proper active device that is suitable for the frequency band of interest, biasing of the active device in order to know the operating point of the device, designing of biasing circuit such that the applied voltage does not affect the performance of the active device,

stability analysis, matching circuits, circuit simulation, tuning and obtaining the required parameters in order to meet the design criteria [11, 13].

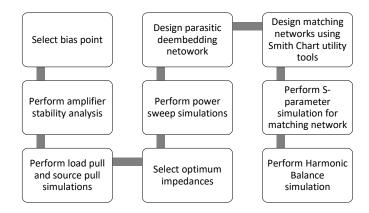


Figure 1. Class-F RFPA design process

3. CIRCUIT DESIGN AND SIMULATION OF CLASS-F RFPA

In this work, a class-F RFPA based on GaN HEMT has been designed and simulated at an operating frequency of 1.5GHz. A 10W GaN HEMT (CGH40010) from Cree is used as an active device. The transistor model for this device is used to realize this work.

3.1. Choice of bias point

Ideal class-F RFPA bias point is usually chosen to be equal to the class B or class AB bias point [13, 14]. In this design, the gate bias voltage Vgs was chosen such that the DC drain current, Ids was around 10 % of the maximum drain saturation current, which is in the deep class AB mode. The drain bias voltage Vds for this device is chosen to be 28 V in order to achieve maximum output power. Therefore, the approximate quiescent drain current was 0.2 A corresponding to quiescent gate voltage of -2.7 V. Figure 2 shows the DC-IV characteristics of the device.

3.2. Amplifier stability analysis

In order to avoid any oscillation in the RFPA design, the stability analysis is performed to the device [13, 15]. Oscillation can cause the gain of the RFPA to increase sharply causing the device to damage. In this paper, parallel resistor and capacitor networks are added into the circuit design to increase the stability in the frequency band of interest. Figure 3 shows the result of the RFPA stability simulation in terms of stability factor K. It is shown that the RFPA is unconditionally stable since the K factor is higher than 1 over a bandwidth of 5 GHz [14, 16]. This demonstrates that the RFPA is stable for the selected operating frequency. In (1, 2) are used since K factor is only defined for two-port networks [17].

$$K = 1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2 \tag{1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2}$$

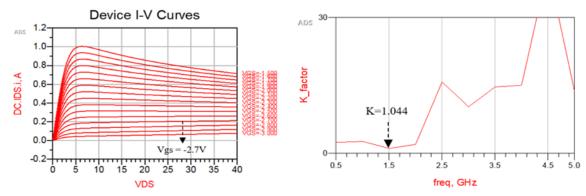


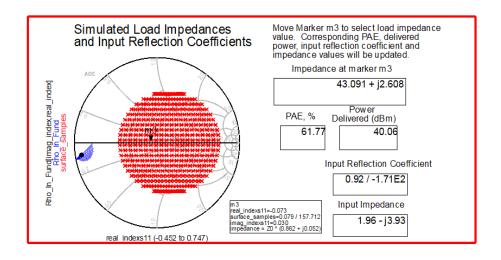
Figure 2. The DC-IV characteristic curve for 10W GaN HEMT (CGH40010)

Figure 3. Graph of K factor versus frequency

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3.3. Load-pull and source-pull analysis

The load-pull and source-pull techniques are used in this work in order to find the optimum impedance at 1.5 GHz [15, 18]. The impedance value obtained from the load-pull simulation is used to design the output matching network whereas the impedance value obtained from source-pull simulation is used to design the input matching network. The load-pull analysis is performed first followed by the source-pull analysis. Load-pull and source-pull simulation can be done in ADS using HB1Tone Load-Pull and HB1Tone Source-Pull design guide. Moreover, the non-linear model is replaced with a large signal model CGH40010 from Cree. Initially, the load impedance value at 1.5 GHz obtained from the device datasheet is used as the fundamental source impedance in the load-pull simulation setup. The second and third-order harmonics are controlled at both input and output for shaping the waveform [16, 19]. Here, the second harmonic impedance is kept at short-circuiting by setting a low impedance while the third harmonic impedance is kept at an open circuit by setting a high impedance. All higher harmonics are closed at 50 Ω . It is observed that the load impedances at the second and third harmonics are crucial to obtain a wide bandwidth, as desired. On the contrary, the load impedance of the fourth harmonic has little effect on bandwidth, while it can be tuned to effectively increase the drain efficiency at the design frequency. The simulator will calculate the PAE and output power for every swept point and generate the PAE and output power contour plot. Figure 4 (a) shows the result for load-pull simulation where a maximum PAE of 61.77 % at approximately 40.06 dBm delivered power is achieved. The optimum load impedance was found at $(43.091 + j2.608) \Omega$. The optimum fundamental source impedance shown in Figure 4 (b) was found to be at $(19.912 + j16.691) \Omega$ with a maximum PAE of 76.41 % at delivered power of 40.72 dBm.



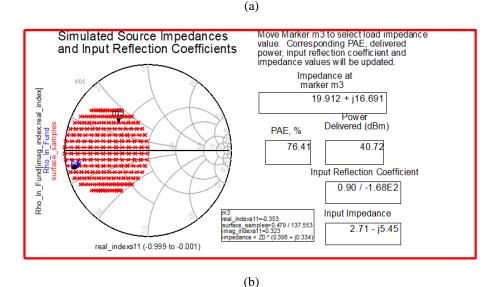


Figure 4. Sweeping region for, (a) Load-pull analysis, (b) Source-pull analysis

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3.4. Parasitic de-embedding network design

The 10W GaN HEMT (CGH40010) device used in this RFPA design comes in a flange type package. This device model includes the package parasitic reactance which consists of passive elements as shown in Figure 5. The current-generator plane shown in Figure 5 is the actual reference plane for the current and the voltage of the device [17, 20]. In order to observe the actual voltage and current waveforms at the current-generator plane, a circuit network which is called the de-embedding network must be applied. Since the current-generator plane is not practically accessible or viewable from outside the package; a mirrored package network with negative values is introduced to cancel out the parasitic elements in the packaged device making the overall structure becomes transparent [18, 21]. The actual measurement plane which is the current-generator plane is now outside the package and the desired voltage and current waveforms can be presented.

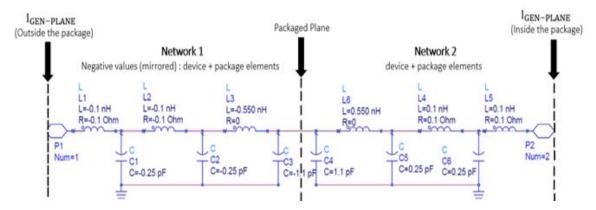


Figure 5. Output de-embedding circuit network

3.5. Input and output matching network design

In a single-stage power amplifier design, it is highly important to design the input and output matching networks. The input matching network (IMN) is used to realize the matching between the input port of the RFPA and the RF source [19, 22]. It is also used to solve the problem of stability and the gain flatness. The output matching network (OMN) is used to achieve the matching between the output port and the load. OMN is designed to achieve the gain and the maximum output power and also to suppress harmonic waves. The matching network in this work is derived from the source-pull and load-pull technique where a high-power transistor's input and output are simultaneously matched in an iterative process, whereas the gain and output power are controlled to achieve maximization. The IMN impedance is obtained from source-pull optimum impedance whereas the OMN impedance is obtained from the load-pull optimum impedance. Smith Chart Utility tool in ADS is used to transform the matching networks into ideal transmission lines where the conjugate matching technique is also applied. The input and output matching networks are also simulated using the S-Parameter simulation tools in ADS to ensure the S11 and S22 are properly matched [20, 23]. The optimized matching networks of the RFPA which consist of open-circuit stubs and quarter-wave transformer are shown in Figure 6 (a) and Figure 6 (b).

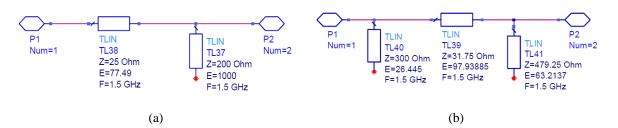


Figure 6. The schematic of, (a) Input matching network, (b) Output matching network after

4. CLASS-F RFPA CIRCUIT DESIGN AND SIMULATION

Towards realizing the final design of class-F RFPA, the ideal transmission line networks are replaced with real microstrip lines [21, 24]. LineCalc tool in ADS is used in order to calculate the length

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and width of microstrip lines. The substrate used for the microstrip lines is FR-4 with a dielectric constant of 4.4 and a thickness of 1.6 mm [22, 25]. The bias-tee composed of the butterfly (MBSTUB) and quarter-wave microstrip transmission lines are used as the DC feed that supplies the gate and the drain of the transistor [23, 26]. As a wideband power amplifier is targeted, microstrip butterfly stubs would be used instead of simple open stubs. Butterflies have a good bandwidth performance and since they have a gradual flaring, the undue effects due to fringing and parasitics are reduced. The ideal DC blocks have been replaced with capacitors whose values are tuned accordingly [24, 27]. The actual capacitor values are also included in this schematic design. The parasitic de-embedding network that is used to observe the waveform is included in the main schematic as the 'OutputTransparentMeasure' block as shown in Figure 7. To verify the operating mode of the designed RFPA, the simulated voltage and current waveforms at the current-generator plane are observed using the harmonic-balance simulator in ADS with operating frequency at 1.5 GHz and input power of 24 dBm. The results of the simulated waveforms at both current-generator plane and package plane are plotted and shown in Figure 8(a) and Figure 8(b). The observed waveforms are similar to that of a standard class-F RFPA which is the half-sinusoidal waveform for drain current and square waveform for drain voltage [25, 28].

The performances of the designed class-F RFPA in terms of gain, output power, bandwidth and efficiency at an operating frequency of 1.5 GHz are illustrated in Figures 9. From Figure 9(a), it is shown that the RFPA delivers a maximum output power of 40.793 dBm at an input power (Pavs) of 24 dBm. The gain of 18dB is achieved at the output power of 40.793 dBm as shown in Figure 9(b). Drain efficiency of 68.37 % in Figure 10(a) and power added efficiency (PAE) of 66.94 % at maximum output power is observed.

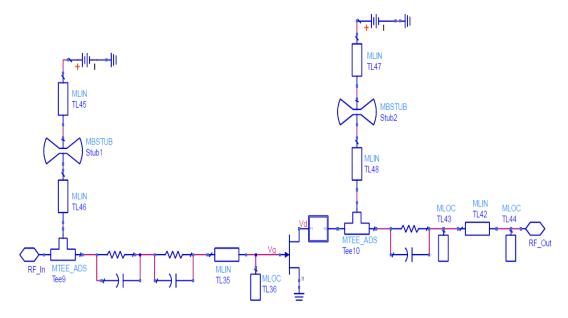


Figure 7. Schematic of the class-F RFPA with biasing circuit

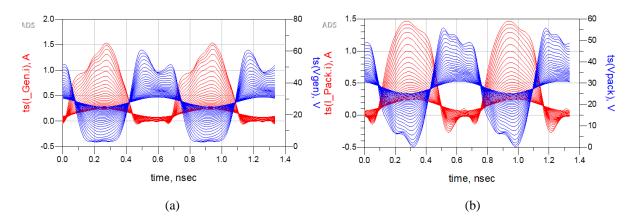


Figure 8. Current and voltage waveforms of the RFPA at, (a) Current-generator plane, (b) Package plane

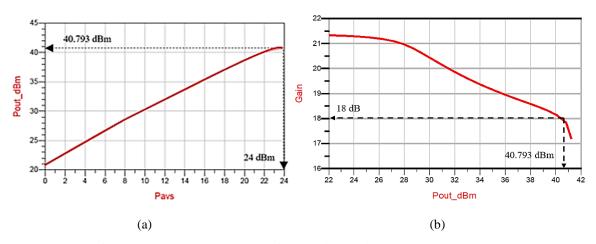


Figure 9. (a) Output power versus input and (b) Gain versus output power

This results from a thorough design step over the entire desired bandwidth where the impedances are successively tuned until the optimum wideband operation is achieved. Moreover, the power added efficiency of 65.0% is achieved at 40.793 dBm of output power as shown in Figure 10(b). A flat gain of 13 dB to 17 dB over a bandwidth of 0.5 GHz to 2.0 GHz is achieved using the S21 simulation as shown in Figure 11. With these results, the design requirements are satisfied.

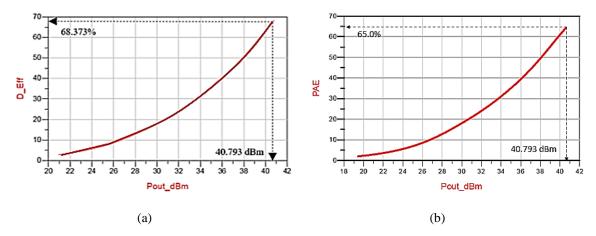


Figure 10. (a) Drain efficiency and (b) Power added efficiency versus output power

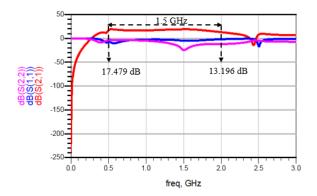


Figure 11. S21, S11 and S22

5. CONCLUSION

In this paper, high flat gain over a bandwidth of $0.5~\mathrm{GHz}$ to $2.0~\mathrm{GHz}$ class-F RFPA based on $10\mathrm{W}$ GaN HEMT (CGH40010) has been designed and simulated. Load-pull and source-pull techniques have been

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applied in order to terminate the first three harmonic impedances to achieve the desired output waveforms. Furthermore, a flat gain response from 13 dB to 17 dB across the desired bandwidth is achieved by applying parallel RC circuits which also works as high pass filters in the matching network. Drain efficiency and PAE of 68.37% and 66.94% respectively were obtained at the maximum output power of 40.79 dBm for an operating frequency of 1.5 GHz. A simple design implementation and efficiency comparable to the other power amplifiers in the literature is also achieved with a wide bandwidth from 0.5 GHz to 2. GHz. It would be possible to achieve even greater gain flatness by increasing the order of the filter, however, at the expense of lower gain. Cost-effectiveness is achieved since the FR4 substrate used in this work is cheaper compared to other substrates. The class-F RFPA designed in this work will be fabricated and tested in order to validate the simulation results.

ACKNOWLEDGEMENTS

The authors would like to acknowledge and thank the MMU management for the MMU Mini Fund grant MMUI/180165 for financing the research.

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BIOGRAPHIES OF AUTHORS



Noor Syakirah Binti Ruslan Hadi was an Electronics Engineering student majoring in Telecommunications from Multimedia University, Cyberjaya. She designed the RFPA for the Final Year Project and received her B.Eng. in Electronics majoring in Telecommunications in 2019. She is currently working as a Project Admin in Fiber department in Binasat Communications Berhad.



Dr Zubaida Yusoff holds the position of a Senior Lecturer at the Faculty of Engineering, Multimedia University. She received her B.Sc. in Electrical and Computer Engineering (cum laude with distinction) and M.Sc. in Electrical Engineering from The Ohio State University, USA in 2000 and 2002 respectively and received Ph.D degree from Cardiff University,UK in 2012. Her teaching and research focuses in the area of Microelectronics, Analog/Mixed Signal RF Circuit Design and Microwave/mm-wave Power Amplifier System.



Md. Golam Sadeque has received B. Sc. Eng. degree in Electrical and Electronics Engineering (EEE) from Rajshahi University of Engineering and Technology (RUET) in 2010. Since 2018, he is pursuing master of engineering science (M. Eng. Sc,) at Multimedia University. His research interest includes design of Radio frequency power amplifier (RFPA) and Biomedical engineering.



Dr. Shaiful J. Hashim is currently an Associate Professor in the Department of Computer and Communication Systems Engineering, Faculty of Engineering, Universiti Putra Malaysia (UPM). He received his Ph. D from Cardiff University, UK (2011), M. Sc from National University of Malaysia (2003) and B.Eng. from University of Birmingham, UK (1998) in the field of Electrical and Electronics Engineering. His research interests include cloud computing, Internet of Things (IoT), network security and non-linear wireless measurement system.



Dr. Muhammad Akmal Chaudhary received the PhD degree in Electrical and Electronics Engineering from Cardiff University, United Kingdom, in September 2011. He was a Postdoctoral Research Associate between October 2011 and September 2012 at the Agilent Centre for High Frequency Engineering, Cardiff University, United Kingdom. At present, he is Associate Professor of Electrical Engineering at Ajman University.