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Modeling of Dirac voltage for highly p-doped graphene field-effect transistor measured at atmospheric pressure

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ABSTRACT

In this paper, the modeling approach of Dirac voltage extraction of highly p-doped graphene field-effect transistor (GFET) measured at atmospheric pressure is presented. The difference of measurement results between atmospheric and vacuum pressures was analyzed. This work was started with actual wafer-scale fabrication of GFET with the purposes of getting functional device and good contact of metal/graphene interface. The output and transfer characteristic curves were measured accordingly to support on GFET functionality and suitability of presented wafer fabrication flow. The Dirac voltage was derived based on the measured output characteristic curve using ambipolar virtual source model parameter extraction methodology. The circuit-level simulation using frequency doubler circuit shows the importance of accurate Dirac voltage value to the device practicality towards design integration.

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1. INTRODUCTION

The deployment of GFET in various design applications is getting more prominent recently as the device gradually picking up its momentum since the inauguration more than a decade ago. For example, GFET is usually found useful for electronic sensing applications thanks to its greater sensitivity and better selectivity [1-3]. Act as a very sensitive material, the device is perfectly fitted for various sensing applications such as physical, biological and chemical sensors. Besides that, GFET is widely employed for integrated circuit designs mostly in the radio frequency (RF) applications with respect to its superior carrier mobilities and high saturation velocity [4-6]. There are limited reports linking GFET with digital and analog mixed signal designs due to the absence of bandgap as well as the relatively low ratio of on-current over off-current [7-9]. Active expansion of circuit design with GFET encouraged further development of full wafer-scale fabrication of the device in order to cope with higher design complexity and chip productivity demands.

The fabrication of GFET at full wafer-scale is not trivial because most of the measured GFET reported in the literatures are generally based on small samples which are applicable for lab-scale researches [10-12]. The significant obstacle to have a fabricated wafer-scale GFET lies in the difficulties of having a uniform large-area graphene layer on top of the silicon wafer. The next challenges in the fabrication flow are to find suitable processes with the available machines in the manufacturing line and to select appropriate chemical during processing steps so that the graphene layer could always preserve its pristine [13]. Another crucial aspect that also needs to be highlighted is the low visibility of single layer graphene on silicon dioxide (SiO_2) layer which will badly affect the design alignment during photolithography step.

There are a few methods proposed in the literatures in order to put graphene layers on top of silicon namely mechanical exfoliation and silicon carbide (SiC) sublimation [14-15]. But for large-area silicon wafer, thermal chemical vapor deposition (CVD) is the best graphene synthesis method for uniformity and effectiveness [16-17]. Although the CVD method could offer such benefits, somehow the quality of graphene being transferred onto the silicon wafer slightly deteriorates especially when the samples are kept at the atmospheric pressure as the graphene layer starts to absorb the water molecules [18-19]. This could be observed during the GFET characterization stage where it acts as a highly p-doped device, resulting to the difficulties in determining the critical Dirac voltage value from the transfer characteristic curves of atmospheric pressure measurement. In order to move back the Dirac voltage from a very positive voltage to its actual pristine properties, the sample must be stored and measured at a very high pressure vacuum environment [12, 20].

Furthermore, Dirac voltage serves as an important parameter during the device setup for circuit-level simulations. Therefore, the Dirac voltage becomes one of the figure-of-merits (FOM) for the designed and fabricated GFET which is typically found in the provided datasheet. In this paper, a methodology of extracting Dirac voltage from the highly p-doped GFET measured at atmospheric environment is proposed. Section 2 presents the wafer-scale fabrication flow of GFET as well as the highlight on the device characterization issues. Section 3 describes the experiment part with related Dirac voltage model extraction flow. Section 4 explains the result and discussion accordingly while section 5 concludes the paper.

2. GFET WAFER-SCALE FABRICATION AND CHARACTERIZATION ISSUES

The starting material for this fabrication work is a p-type silicon substrate with boron as dopant at the doping concentration of $1x10^{15}$ cm^{-3}. The back-gate GFET was fabricated on commercially available monolayer graphene on SiO_2/Si substrate at 4-inch wafer size [21, 22]. The graphene layer was grown by thermal CVD method and transferred to 300 nm thickness of SiO_2/Si substrate. In order to build the GFET structure on top of the graphene on silicon wafer, three layers of chrome photolithography mask were tape-out accordingly for photoresist (PR) fiducial mark, graphene channel definition and source/drain (S/D) contact.

At the beginning, with the availability of commercial graphene on silicon wafer, fabrication process was started with a deposition of positive PR for the first mask namely fiducial alignment mark. The creation of this alignment mark is vital considering the fact that the starting surface is a clear monolayer graphene from the supplier without any mark on it. The PR was then exposed and developed to have the important alignment mark pattern on the substrate. Next, the graphene and SiO_2 layers were etched respectively, using oxygen plasma and fluorine-based chemistry. In order to improve visibility of the alignment mark for the second mask patterning, the silicon layer was further etched using deep reactive-ion etching (DRIE) machine. After that, the PR was removed and water cleansed using acetone/isopropyl alcohol (IPA) process.

In the second mask, the graphene channel structure was identified utilizing a positive PR. The PR was spin-coated at targeted resist thickness of 1.5 to 2 um. After expose and develop procedures, the graphene layer was then etched using oxygen plasma where all graphene area was removed except the area covered by PR. Once the graphene channel etch has completed, the PR was again stripped and water cleansed using acetone/IPA process. For the third mask, the negative PR was spin-coated onto the wafer as the S/D contact patterning was performed by a lift-off process. The S/D metal deposition was done by RF sputter where 5 nm titanium (Ti) and 40 nm gold (Au) contacts evaporated on the wafer. This was followed by metal lift-off procedure where the wafer was put in TechniStrip NI555 PR stripper for about 12 to 14 hours. The process was completed with annealing treatment in ambient environment for 3 minutes at 100˚C.

Besides the S/D metal contacts that represent the source and drain terminals accordingly, the silicon substrate of the fabricated back-gate GFET then acts as a gate terminal. After completing with GFET fabrication, the next step is towards the device characterization where there are some issues that need to be addressed. Firstly, the device is very sensitive to the surrounding environment, especially to the water molecules [12]. The strong reaction with water molecules contributed negatively to the GFET characteristics such as difficulties in Dirac voltage determination, higher contact resistance and lower carrier mobility. Secondly, due to the fact that the Dirac voltage has been shifted more towards a very positive bias, therefore the measurement at atmospheric environment only would not be able to detect such unique behavior of pristine graphene. Instead of normal atmospheric pressure measurement, the device needs to be measured using advanced high pressure vacuum environment so that graphene material could reach back to its pristine state and related Dirac voltage value could be measured. It was reported that the contact resistance value measured at a high vacuum environment is 35% lower compared to the measurement at open air which further supports that inert atmosphere would also change the carrier mobility and Dirac voltage values [11].

3. EXPERIMENT

The output and transfer characteristic curves of the fabricated GFET were measured using Agilent B1500A semiconductor device analyzer. The output characteristic curve or drain current versus drain voltage (I_d-V_d) plot is required to show that there is a good metal to graphene contact so that it could perform a general transistor function. Besides that, the I_d-V_d plot also provides some insight on the contact resistance and S/D graphene channel sheet resistance values. On the other hand, the transfer characteristic curve or drain current versus drain voltage (I_d-V_g) plot is necessary for the extraction of Dirac voltage value. The main hurdle in this work is the absence of wafer prober with high vacuum pressure which is required to preserve the pristine graphene behavior. Therefore, the micro probing work was done using standard open air atmospheric pressure wafer prober attached with the device analyzer. With such measurement system setup, it was expected that it is difficult to determine the critical Dirac voltage parameter. In order to overcome the obstacle, the modeling approach of determining the Dirac voltage using atmospheric pressure measurement data was proposed as shown in Figure 1.

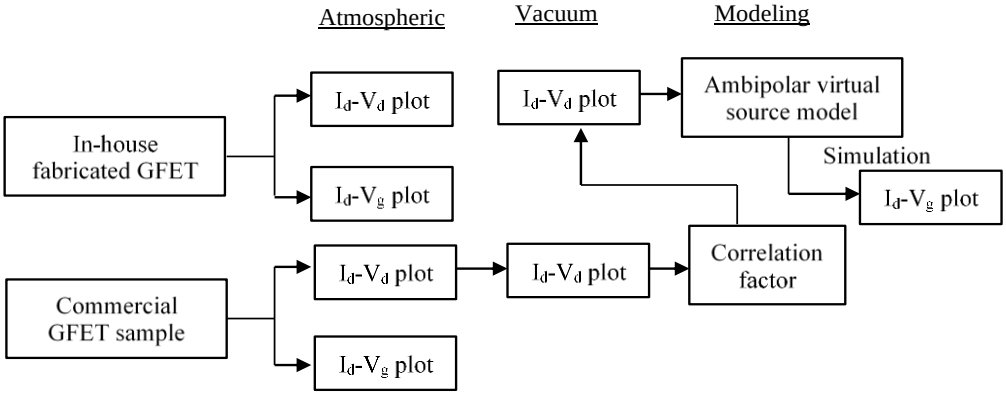


Figure 1. Model extraction flow for in-house fabricated GFET

Initially, the I_d-V_d and I_d-V_g plots of in-house fabricated GFET were measured for the characterization data at atmospheric environment. Next, the same plots were measured using the commercial GFET which acts as a benchmarking sample. The commercial sample was purchased from the same supplier which also provides the CVD graphene on silicon wafer so that there is a close correlation in term of graphene quality produced [22]. A correlation factor was then derived by determining the differences between I_d-V_d plots measured at atmospheric and vacuum pressures where the curve of output characteristic in vacuum condition was provided in the sample's datasheet. The measurement of I_d-V_d plot at atmospheric condition for internally fabricated GFET was then projected to vacuum condition plot using the percentage input of the derived correlation factor. In order to determine the elusive Dirac point from I_d-V_g plot, the projected I_d-V_d data was ported into physic-based ambipolar virtual source model parameter extraction [23]. This ambipolar virtual source model provides an accurate insight into GFET physics as it caters for both static transport and dynamic models where the drain current formula is given by

$$I_d = ((Q_{elec} + Q_{hole}) \text{ x } v_{x0} \text{ x } F_{sat}) \text{ x } W \quad (1)$$

where Q_{elec} and Q_{hole} are for electron and hole concentration respectively, v_{x0} is carrier injection velocity, F_{sat} is an empirical function of transport model and W is the channel width. This model is suitable for Dirac voltage estimation where the terminal voltages for electron (V_{tn}) and hole (V_{tp}) are given by

$$V_{tn} = V_{min0} + \text{delta} \quad (2)$$

$$V_{tp} = V_{min0} - \text{delta} \quad (3)$$

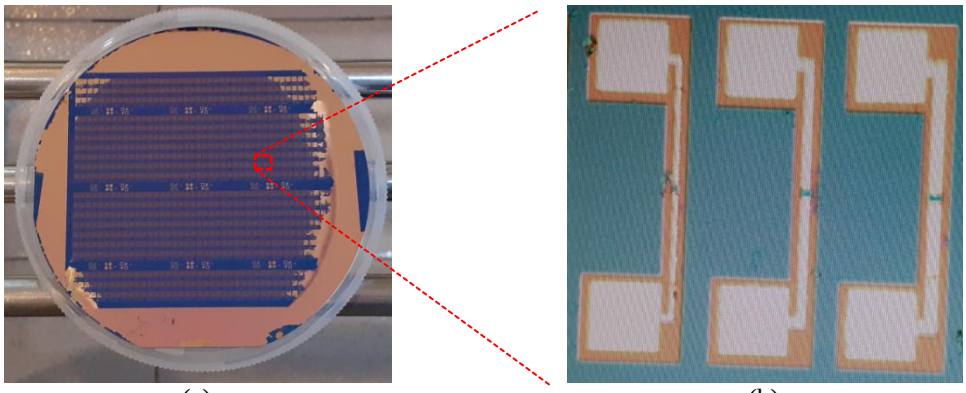
where delta stands for the shift in threshold voltage for charge trapping and V_{min0} is referring to the Dirac voltage point. This work takes the advantages of compact and comprehensive physic-based approach of the ambipolar virtual source model to determine the Dirac voltage value by performing the model curve fitting and model parameter extraction using measured and projected I_d-V_d data. From the extracted model

parameters, the I_d-V_g plot was simulated using commercial Spectre simulator in order to generate the transfer curve with ambipolar characteristics. The extracted GFET model was also simulated using the frequency doublers circuit to show its suitability for design integration and evidence the significance of graphene-based transistor compared to silicon-based devices.

4. RESULTS AND DISCUSSION

4.1. Output and transfer characteristic curves

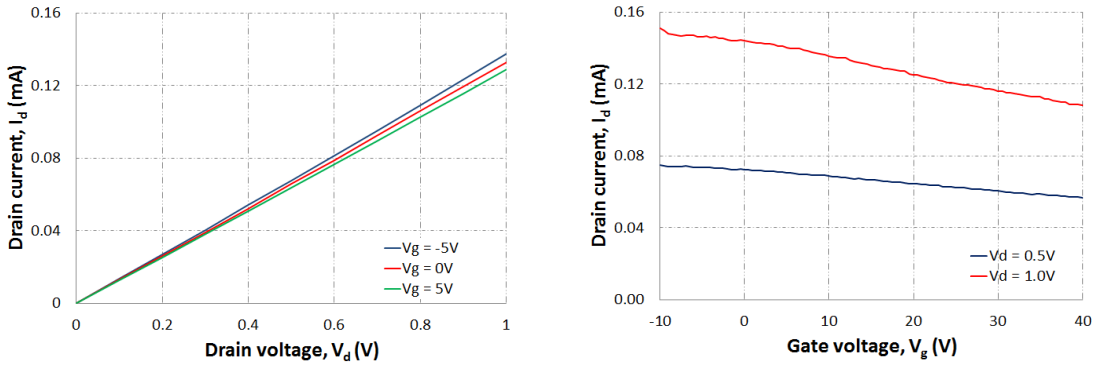
The photograph of finished back-gate GFET on 4-inch wafer is shown in Figure 2(a). Apart from a few lines reserved for alignment mark identification, the rest is actually a sea-of-graphene-based transistors printed during the full wafer-scale fabrication work. Figure 2(b) displays the zoomed-in picture of a few GFETs which basically contain graphene channel in the middle connected to the symmetrical source and drain terminals while the gate terminal located at the back side of the wafer.



(a) (b)

Figure 2. Picture of fabricated 4-inch wafer, (a) Finished wafer, (b) Close view of a few GFETs

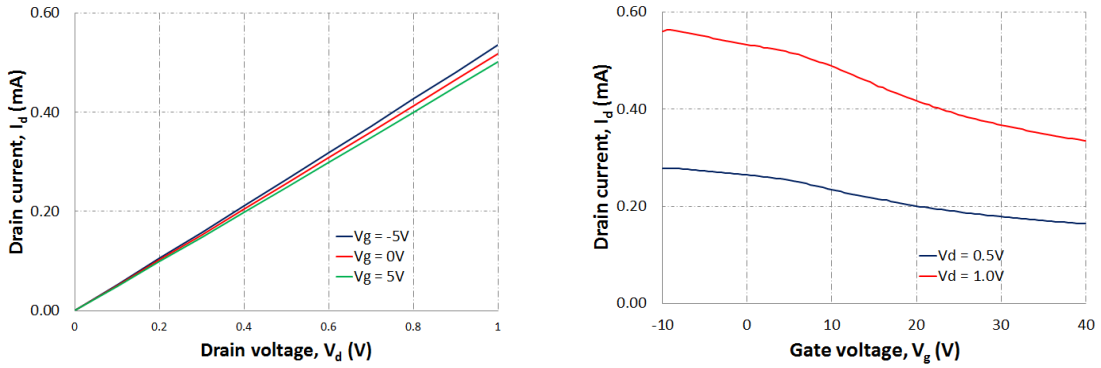
The measured I_d-V_d and I_d-V_g plots from the fabricated GFET are presented respectively in Figure 3(a) and 3(b) for gate length (L) of 5 um and gate width (W) of 10 um. For I_d-V_d plot, the drain current values are measured at various gate voltages (V_g) from -5V to 0V and 5V to figure out that the fabricated device is either n-type or p-type [24]. The sheet resistance value is derived by dividing extracted resistance value from the I_d-V_d plot to the number of square value which in this case is W/L. The curves show that the fabricated GFET is a p-type device as the drain current from the negative gate voltage is higher compared to the drain current from positive gate voltage. Besides that, the resistor-like I_d-V_d plot also shows that the sheet resistance value of graphene channel is about 3700 Ω/□, which is considered as a reasonable figure for graphene devices and indicates that the graphene/metal interface is in a fine condition [25]. The linearly increases of drain current with drain voltage (V_d) are critical to show that there is a good contact between graphene/metal or else the measurement will just exhibit as an open or short device characteristic.



(a) (b)

Figure 3. Measurement results from the fabricated wafer, (a) I_d-V_d plot, (b) I_d-V_g plot

For I_d-V_g plot, the gate voltage is swept from -10V to 40V, which is the maximum supplied voltage of the Agilent B1500A available in this work and drain voltages are set at 0.5V and 1V. The result shows that there is no Dirac voltage found even when the gate voltage was ramped up to 40V to suggest that the fabricated GFET is a very highly p-doped device. The Dirac voltage has been shifted to a very high gate voltage value as the measurement is performed at atmospheric pressure in the absence of high-end high vacuum pressure wafer probing system. The same result found in the measurement at atmospheric pressure using commercial sample where there is no ambipolar characteristic could be observed as shown in Figure 4 for GFET with L=50 um and W=50 um. It is worth mentioning that the availability of different GFET dimensions (L and W) between in-house fabricated and commercial sample has certainly made a significant difference for the derivation of graphene channel sheet resistance value [11].

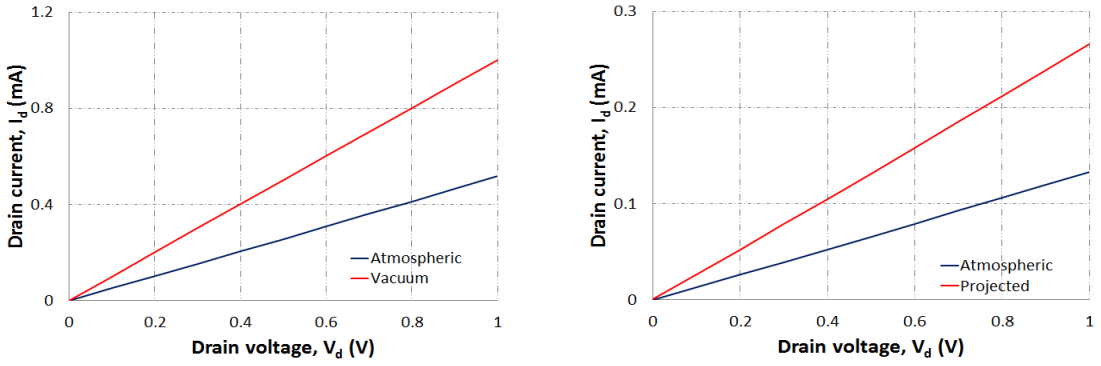


(a) (b)

Figure 4. Measurement results from commercial GFET sample, (a) I_d-V_d plot, (b) I_d-V_g plot

4.2. Modeling of Dirac voltage

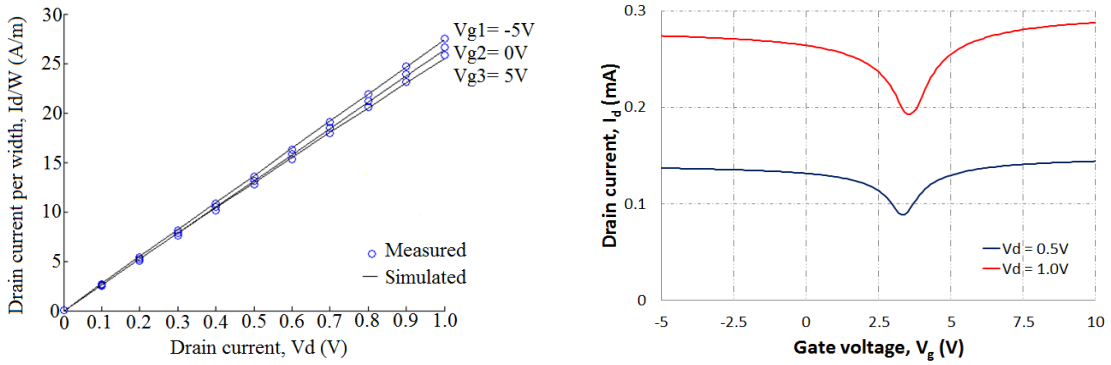
The comparison between measurement data at atmospheric and vacuum pressures for the commercial GFET sample is shown in Figure 5(a) where the high vacuum pressure data are extracted from the provided product datasheet. It is discovered that there is about 50% divergence from atmosphere to high vacuum pressure measurement understandably due to water molecule absorption by the graphene material at atmospheric pressure, which has increased the contact resistance, reduced the drain current and shifted that Dirac point towards very positive gate voltage. Figure 5(a) shows the sheet resistance values in atmospheric environment is at 2000 Ω/□ while in vacuum environment is at 1000 Ω/□. With the assumption that the same deviation would be observed due to the fact that both graphene on silicon wafer in this work and commercial GFET sample are produced by the same supplier using a similar CVD method, the measurement data at vacuum pressure is projected at 50% increase from the fabricated GFET measurement of standard atmospheric pressure as shown in Figure 5(b). In that respect, with the introduction of related correlation factor, the sheet resistance projected at high vacuum environment is extracted at 1800 Ω/□.



(a) (b)

Figure 5. Comparison between measurement at atmospheric and vacuum pressures, (a) Commercial GFET sample, (b) Fabricated GFET wafer

From the derivation of experimental data at vacuum pressure, the SPICE-like model parameters for the in-house fabricated GFET are extracted using MATLAB parameter extraction tool and the comparison between measured and simulated data is shown in Figure 6(a). The result proves that the ambipolar virtual source model is able to accurately model the provided measurement data as supported by the close curve fit of I_d-V_d plot where the carrier mobility and Dirac voltage are extracted respectively at 1500 cm^2/V.s and 3.11V. Figure 6(b) illustrates the I_d-V_g plot simulated using Spectre simulator with ambipolar characteristic found at around the Dirac point. These results show that extraction of Dirac voltage value of highly p-doped GFET using measurement data at atmospheric pressure is possible with the capability of compact and physic-based ambipolar virtual source model.



(a) (b)

Figure 6. Modeling of Dirac voltage of the fabricated GFET wafer, (a) Curve fit between measured and simulated data from I_d-V_d plot, (b) Simulation of I_d-V_g plot using Spectre simulator

4.3. Circuit-level simulation

Frequency doubler circuit using graphene-based technology performs as the same function of full wave rectifier using silicon-based technology for multiplying the output frequency [26]. While full wave rectifier requires more than a single device to execute the task, frequency doubler in graphene-based technology only needs a single GFET with respect to its ambipolar capability. In order to express the suitability of the in-house fabricated GFET into the design application, the frequency doubler circuit as shown in Figure 7 is utilized accordingly. This circuit-level simulation is also performed using Spectre simulator where circuit netlist is extracted prior to the simulation work. One of the important steps in simulating the circuit is to supply a correct bias to the gate voltage (V_g) which is in this case is the Dirac voltage value. Figure 8(a) displays the input sine wave at the frequency of 1 kHz supplied to the gate terminal of the GFET. Figure 8(b) and 8(c) show the output signal from the drain terminal when V_g is biased correspondingly at smaller (2V) and greater (4V) than the Dirac voltage, where both setups were not able to increase the output frequency. On the other hand, only with used of previously extracted Dirac voltage, the circuit managed to generate the output signal at the frequency of 2 kHz as shown in Figure 8(d), which has matched its design purpose.

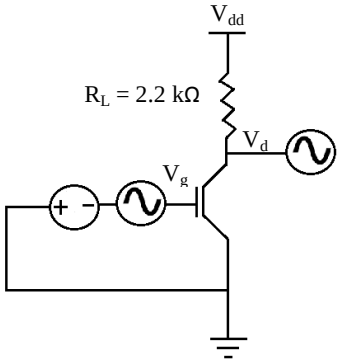


Figure 7. GFET circuit-level application using frequency doubler circuit

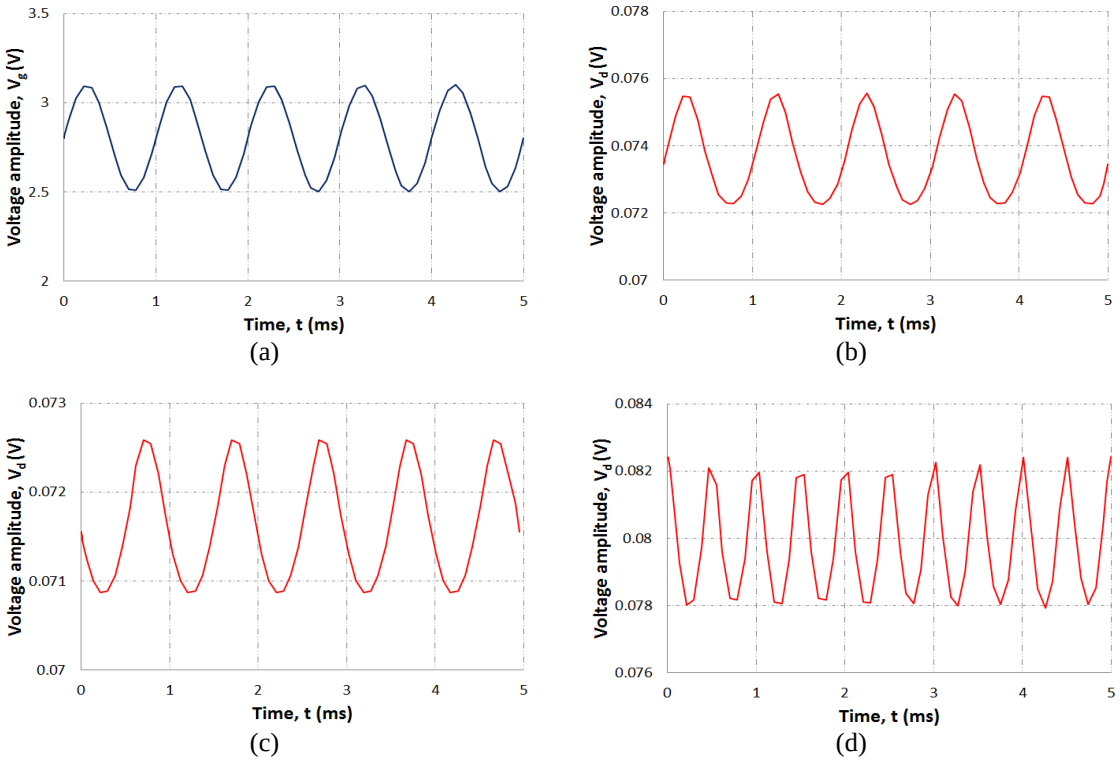


Figure 8. Circuit simulation results, (a) Input signal, (b) Output signal at Vg<Dirac voltage, (c) Output signal at Vg>Dirac voltage, (d) Output signal at Vg=Dirac voltage

5. CONCLUSION

The modeling approach of Dirac voltage extraction from highly p-doped GFET measured at atmospheric environment has been presented. The normal resistor-like output characteristic curve measurement from in-house fabricated GFET reveals that the device is workable and the contact of metal/graphene interface is good. The transfer characteristic curve measurement at atmospheric environment with no Dirac voltage found suggests that fabricated device is highly p-doped as the wafer is exposed to open air over the time. With the availability of correlation factor based on the benchmarked commercial sample, the output characteristic curves have been projected for measurement data at high vacuum pressure environment. Backed by the capability of physic-based ambipolar virtual source model extraction methodology, the Dirac voltage has been extracted and observed even in the absence of high vacuum pressure wafer probing facility. The successful implementation of extracted GFET model parameters into the frequency doubler circuit using commercial Spectre simulator shows that circuit design integration is possible and advantageous, especially with unique ambipolar capabilities which are not offered by common CMOS transistors.

REFERENCES

[1] B. Zhan, C. Li, J. Yang, G. Jenkins, W. Huang, and X .Dong, "Graphene field-effect transistor and its application for electronic sensing," *Small*, vol. 10, no. 20, pp. 4042-4065, 2014.
[2] A. K. Manoharan, S. Chinnathambi, R. Jayavel, and N. Hanagata, "Simplified detection of the hybridized DNA using a graphene field effect transistor," *Sci. and Tech. of Advanced Material*, vol. 18, no. 1, pp. 43-50, 2017.
[3] S. Dana and M. M. Varma, "Gas-selective signal amplification in fluctuation-based graphene FET sensors," *IEEE Sensors Journal*, vol. 16, no. 17, pp. 6533-6536, 2016.
[4] N. Petrone, I. Meric, T. Chari, K. L. Shepard, and J. Hone, "Graphene field-effect transistors for radio-frequency flexible electronics," *Journal of The Electron Device Society*, vol. 3, no. 1, pp. 44-48, 2015.
[5] M. A. Andersson, Y. Zhang, and J. Stake, "A 185-215-GHz subharmonic resistive graphene FET integrated mixer on silicon," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 165-172, 2017.
[6] H. J. Lee and J. G. Yook, "Graphene nanomaterials-based radio-frequency/microwave biosensors for biomaterials detection," *Materials*, vol. 12, no. 6, pp. 1-13, 2019.
[7] M. S. Jang, H. Kim, Y-W. Son, H. A. Atwater, and W. A. Goddard, "Graphene field effect transistor without an energy gap," *Proceedings of the National Academy of Sciences*, vol. 10, no. 22, pp. 8786-8789, 2013.
[8] A. Safari, M. Dousti, and M. B. Tavakoli, "Monolayer graphene field effect transistor based operational amplifier," *Journal of Circuits, Systems and Computers*, vol. 28, no. 3, pp. 1-15, 2019.

[9] F. Ke, Y. Chen, K. Yin, J. Yan, H. Zhang, Z. Liu, S. T. John, J. Wu, H-K. Mao, and B. Chen, "Large bandgap of pressurized trilayer graphene," *Proc. of the National Academy of Sciences*, vol. 116, no. 19, pp. 9186-9190, 2019.
[10] R. C. Ordonez, C. K. Hayashi, C. M. Torres, J. L. Melcher, N. Kamin, G. Severa, and D. Garmire, "Rapid fabrication of graphene field-effect transistors with liquid-metal interconnects and electrolytic gate dielectric made of honey," *Scientific Reports*, vol. 7, no. 1, pp. 1-9, 2017.
[11] F. Guibileo, A. D. Bartolomeo, N. Martucciello, F. Romeo, L. Lemmo, P. Romano, and M. Passacantando, "Contact resistance and channel conductance of graphene field-effect transistors under low-energy electron irradiation," *Nanomaterials*, vol. 6, no. 11, pp. 1-9, 2016.
[12] D. H. Tien, J-Y. Park, K. B. Kim, N. Lee, and Y. Seo, "Characterization of graphene-based FET fabricated using a shadow mask," *Scientific Reports*, vol. 6, no. 1, pp. 1-8, 2016.
[13] L. Liao and X. Duan, "Graphene for radio frequency," *Materials Today*, vol. 15, no. 7-8, pp. 328-338, 2012.
[14] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Prog. Article in Nature Materials*, vol. 6, pp. 183-191, 2007.
[15] W. A. de Heer, C. Berger, M. Ruan, M. Sprinkle, X. Li, Y. Hu, B. Zhang, J. Hankinson, and E. Conrad, "Large area and structured epitaxial graphene produced by confinement controlled sublimation of silicon carbide," *Proc. of the National Academy of Sciences*, vol. 108, mo. 41, pp. 16900-16905, 2011.
[16] A. Yakubu, S. G. Danjumma, and Z. Abbas, "Graphene synthesis by chemical vapour deposition (CVD): A review on growth mechanism and techniques," *Int. J. of Eng. Research and Technology*, vol. 8, no. 5, pp. 15-26, 2019.
[17] C. Shen, X. Yan, F. Qing, X. Niu, R. Stehle, S. S. Mao, W. Zhang, and X. Li, "Criteria for the growth of large-area adlayer-free monolayer graphene films by chemical vapor deposition," *J. of Materio.*, vol. 5, no. 3, pp. 463-470, 2019.
[18] Z. Eres and S. Hrabar, "Low-cost synthesis of high-quality graphene in do-it-yourself CVD reactor," *Automatika*, vol. 59, no. 3-4, pp. 254-260, 2018.
[19] C. Melios, C. E. Giusca. V. Panchal, and O. Kazakova, "Water on graphene: Review of recent progress," *2D Mater*, vol. 5, pp. 1-18, 2018.
[20] Y. Yang, K. Bremmer, and R. Murali, "The influence of atmosphere on electrical transport in graphene," *Carbon*, vol. 50, no. 5, pp. 1727-1733, 2012.
[21] L. Anzi, A. Mansouri, P. Pedrinazzi, E. Guerriero, M. Fiocco, A. Pesquera, A. Centeno, A. Zurutuza, A. Behnam, E. A. Carrion, E. Pop, and R. Sordan, "Ultra-low contact resistance in graphene devices at Dirac point," *2D Mater*, vol. 5, no. 2, pp. 1-8, 2018.
[22] K. Asadi, E. C. Timmering, T. C. T. Geuns, A. Pesquera, A. Centeno, A. Zurutuza, J. H. Klootwijk, P. W. M. Blom, and D. M. de Leeuw, "Up-scaling graphene electronics by reproducible metal-graphene contacts," *ACS Appl. Mater. Interfaces*, vol. 7, no. 18, pp. 9429-9435, 2015.
[23] S. Rakheja, Y. Wu, H. Wang, T. Palacios, P. Avouris, and D. A. Antoniadis, "An Ambipolar virtual-source-based charge-current compact model for nanoscale graphene transistors," *IEEE Trans. on Nanotech.*, vol. 13, no. 5, pp. 1005-1013, 2014.
[24] X. S. Li, Z. Deng, Z. Chen, and Q. Fei, "Analysis and simplification of three-dimensional space vector PWM for three-phase four-leg inverters," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 450-464, 2011.
[25] A. D. Bartolomeo, F. Giunileo, L. Lemmo, F. Romero, S. Santandrea, and U. Gambardella, "Transfer characteristics and contact resistance in Ni- and Ti-contacted graphene-based field-effect transistors," *Journal of Physics: Condensed Matter*, vol. 25, no. 15, pp. 1-6, 2013.
[26] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multipliers," *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 547-549, 2009.

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