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Improved performance with fractional order control for asymmetrical cascaded H-bridge multilevel inverter

Vemula Anil Kumar, Arounassalame Mouttou
Department of Electrical and Electronics Engineering, Pondicherry Engineering College, India

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ABSTRACT

This paper proposes a control scheme for seven level asymmetrical cascaded H-bridge multi level inverter (ACHBMLI) based on fractional order calculus. The seven level ACHBMLI consists of two H-bridges that are connected in series and are excited by different dc voltage sources. A simplified model is developed by assuming the small signal variation component is equal in both the H-bridges. A fractional order PID (FO-PID) controller is designed for the ACHBMLI using the simplified model. Simulation study shows the adequacy of FO-PID controller in giving an output voltage with minimum distortions. A conventional PID controller is also designed for ACHBMLI using the same simplified model. The performance of the ACHBMLI with FO-PID controller is compared with the performance of ACHBMLI with conventional PID controller. The simulation results prove the superiority of FO-PID controller in maintaining the output voltage of the ACHBMLI close to the reference voltage and in reducing the harmonic distortion of output voltage of the inverter. The simulation was done using MATLAB and the parameters of FO-PID controller was designed using FOMCON tool box.

Corresponding Author:

Vemula Anil Kumar,
Department of Electrical and Electronics Engineering,
Pondicherry Engineering college,
Pondicherry, India.
Email: vemula_anil@yahoo.co.in

1. INTRODUCTION

Multilevel inverter is a power electronic circuit that provides the required ac output by using an input of multiple low level DC voltages. The aim is to create a staircase yield voltage using isolated DC voltage resources as inputs. A sinusoidal waveform can be achieved using multiple output levels which can be obtained through multi level inverters (MLIs). Because of their features such as superior electromagnetic capability, low switching losses, and low harmonics, MLIs have received increasing attention recently, especially in high power applications. Due to their switching frequencies, decreased use of output filters, MLI topologies at the same power ratings, have advantages over two level inverter topologies [1-2]. Cascaded H-Bridge MLIs (CHBMLIs) has many advantages such as low harmonics, reduced number of switches, reduced circuit complexity, less size and cost, etc. Thus CHBMLIs can be used in applications dealing with renewable energy sources like photovoltaic cells, fuel cells. Cascaded multi level inverter can have symmetrical and asymmetrical structure. These two types of CHBMLIs can be used to create a required yield voltage from different DC voltage sources [3-4]. If the isolated voltage sources connected to each H-bridge are identical, the structure is symmetrical. However, if the isolated voltage sources are unequal in magnitude the structure is asymmetrical.

The multi carrier PWM technique is an effective method to control an asymmetrical MLI. In this PWM technique a carrier wave (high-frequency) is compared with reference wave (low-frequency) [5-7].

In this present study, multicarrier modulation is realized through level shifted techniques known as alternate phase opposition disposition (APOD), phase opposition disposition (POD), phase disposition (PD) [8-9].

Although the performance of the inverter is satisfactory in the absence of load variations, closed loop operation is required when the performance of the system is degraded due to sudden changes in load. A conventional integer order- PID controller is an ideal choice for any dynamic system to implement closed loop control. The drawbacks associated with conventional PID controllers are limited tuning parameters, lack of robustness, etc. A fractional PID controller which has additional tuning parameter provides robustness under closed loop operation [10-12].This study compares performance of a seven level asymmetrical CHBMLI under open-loop operation with conventional PID controller and closed-loop operations with FO-PID controller. To design a controller it is necessary to derive the mathematical model of the system. This paper also explains the small signal modelling of inverter to carry out the design of a controller [13]. The fractional order controller is designed using FOMCON tool box. The subsequent sections of this paper describe proposed closed loop operation of ACHBMLI, detailed methodology using small signal model of seven level ACHBMLI, modulation strategy, design of fractional order PID controller, simulation results and conclusions.

2. PROPOSED METHOD

Figure 1 shows the block diagram of proposed control scheme for seven levels Asymmetrical cascaded H-Bridge multilevel inverter (ACHBMLI). Here Fractional order -PI controller is used as a controller to maintain the output voltage of the inverter constant and to reduce the total harmonic distortions. Different level shifted multi carrier PWM techniques are used to analyse the performance of the proposed system.

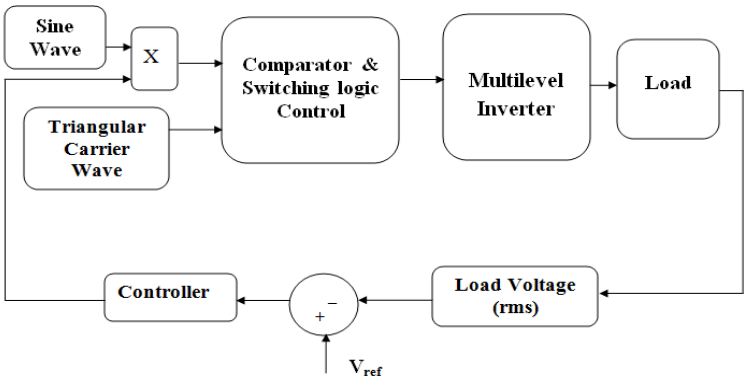


Figure 1. Block diagram proposed system

3. RESEARCH METHOD

In order to design a suitable controller it is very important to develop a small signal model of the inverter which is a transfer function that relates output voltage and switching function [14-15].

3.1. Small signal modelling of seven level ACHBMLI

Figure 2 shows the seven levels ACHBMLI with an LC filter. It has two series-connected H-bridge converters [16]. The terminal voltage of each module is multiplication of DC-link voltage and the switching function u(t). By applying Kirchhoff`s laws in the circuit in Figure 2.

$$L\frac{di(t)}{dt}+v(t)=u_1(t)Vdc_1+u_2(t)Vdc_2 \quad (1)$$

$$i_c(t)=i(t)-i_{Load}(t)=i(t)-\frac{v(t)}{R} \quad (2)$$

The right side of (1) can be written as (3).

$$u_1(t)V_{dc1}+u_2(t)V_{dc2}=g(t) \quad (3)$$

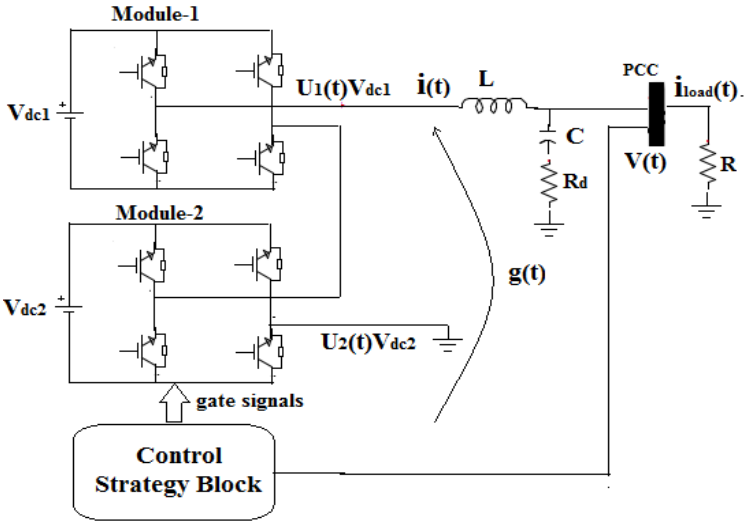


Figure 2. Asymmetrical CHBMLI

The capacitor current is written as:

$$i_c(t) = C\frac{dv(t)}{dt} - C\frac{dR_d i_c(t)}{dt} \tag{4}$$

Substitute (2) into (4), we can get (5):

$$i(t) - \frac{v(t)}{R} = C\frac{dv(t)}{dt} - C\frac{dR_d(i(t) - i_{Load}(t))}{dt} \tag{5}$$

The current $i(t)$ is obtained by isolating $i(t)$ in (1), as given by (6):

$$i(t) = \int \frac{g(t)}{L}dt - \int \frac{v(t)}{L}dt \tag{6}$$

Substitute (6) in (5) and differentiating both sides we will get (7):

$$\frac{g(t)}{L} + \frac{CR_d}{L}\frac{dg(t)}{dt} = C\frac{d^2v(t)}{dt^2} - \frac{CR_d}{R}\frac{d^2v(t)}{dt^2} + \frac{1}{R}\frac{dv(t)}{dt} + \frac{CR_d}{L}\frac{dv(t)}{dt} + \frac{v(t)}{L} \tag{7}$$

Because of non linear nature of (7) due to switching function, v*(t) & u(t)* are changed by a fixed value added to a small signal component which are shown in (8)-(9):

$$v(t) = \overline{V} + \bar{v}(t) \tag{8}$$

$$u(t) = \overline{U} + \bar{u}(t) \tag{9}$$

Substitute (8) and (9) in (7) and taking laplace transform, we can get the transfer function as shown in (10)

$$\frac{\overline{V}(s)}{\overline{U}(s)} = G_v(s) = \frac{(1 + CR_d s)\sum_{k=1}^{2} V_{dck}}{s^2\left(LC + \frac{LCR_d}{R}\right) + s\left(CR_d + \frac{L}{R}\right) + 1} \tag{10}$$

Equation (10) represents the simplified small signal model of seven level ACHBMLI. This transfer function model can be used for the design of controller.

3.2. Modulation strategy

There exist various modulation techniques to generate pulses for the switches of an MLI [17-19]. In this study, bipolar multicarrier level-shifted PWM techniques are considered for analysis. In these techniques, one reference signal and (n-1) carrier signals are used to create n levels at the yield of the inverter. Thus, one reference and six carriers are required to generate seven levels in the yield of the seven-level asymmetrical CHBMLI. All the carriers are vertically disposed and arranged to get various level shifted pulses. The carrier arrangement in PD-PWM is in-phase. However, in POD-PWM, the carriers are 180° out of phase above and below the reference axis. In APOD-PWM, the carriers are 180° out of phase alternatively [20-21]. The frequency (f_c) and amplitude (V_c) of carrier signals are same in each of the aforementioned three cases. The modulation index (m_a) and frequency index (m_f), which are used to define the modulation of output signals, are expressed as follows:

$$m_a = \frac{2V_m}{(n-1)V_c}; \qquad m_f = \frac{f_c}{f_m} \tag{11}$$

where V_m and V_c represent the amplitude of the modulating and carrier signals, respectively, and n gives the levels in the output [22-23].

3.3. Design of fractional order PID controller

The small signal model of the inverter with control strategy is presented in Figure 3. Here the loop is composed of a fractional order PID, multi carrier level shifted pulse width modulator and the small-signal model. The controller in this methodology can be accurately designed to such an extent that the controller causes the yield voltage to pursue the reference without a steady-state error [24]. The parameters of the ACHBMLI used for the present study is given in Table 1.

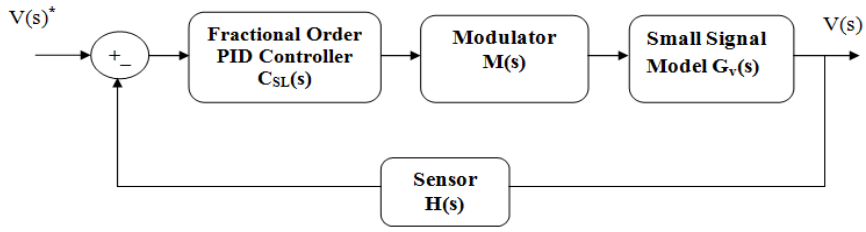


Figure 3. Voltage control scheme

The transfer function of open loop system excluding the controller is shown by (12).

$$A(s)=H(s)M(s)G_V(s) \tag{12}$$

The transfer function $G_v(s)$ is given in (10). The transfer function of modulator can be considered as one. The open loop system transfer function including the controller is shown by (13).

$$Q(s)=C_{SL}(s)M(s)H(s)G_V(s)=C_{SL}(s)A(s) \tag{13}$$

Conventional integer order PID controller (IO-PID) is an ideal choice for any dynamic system to implement closed loop control. However, the drawbacks associated with conventional PID controllers are limited tuning parameters and lack of robustness. A fractional PID controller (FO-PID), which has additional tuning parameters, provides robustness under closed loop operation. FOPID controller has two additional parameters λ and μ in addition to K_p,K_i,K_d to tune, and it is the main reason behind the prevalence of FO-PID's to integer order PID's. So $PI^{\lambda}D^{\mu}$ controller may upgrade the system control execution [24]. The FO-PID transfer function is given by:

$$C_{SL}(s) = K_P + \frac{K_I}{s^{\lambda}} + K_D s^{\mu}\text{; Where } \lambda \text{ and } \mu > 0. \tag{14}$$

To design a controller of the form given in (14) the requirements considering for the dynamic response of the ACHBMLI is given in Table 2.

Table 1. Parameters of system

Parameter	Value
Voltage of module-1(V_{dc1})	120V
Voltage of module-1(V_{dc2})	240V
Load resistance(R)	50 Ohm
LC filter	L=4.25mH ,C=5µF
Fundamental frequency	50Hz
RMS value of voltage reference	230V
Sensor gain	1/360

Table 2. Dynamic response requirements

Quantity	Value
Desired cut-off frequency	2 KHz
Desired Phase margin	60^0

FOMCON tool box is used to calculate and optimize the parameters of FO-PID controller [25]. This tool provide for identifying the process by the models(FOPDT, IPDT, FOIPDT) and calculating gains of IO-PID controller using Ziegler-Nichols tuning strategy. The parameters of PID are initially set to $K_p=K_i=K_d=50$, $\lambda=\mu=1$. Initially to design integer order PID controller the exponents are fixed. For gains the search limits are set to K=[−400; 400] and γ=[0.01; 1]. The refined Oustaloup filter approximation is used for simulation. Phase margin is set to 60 degrees (non-strict). Performance metric is integral of square error (ISE). The following integer order PID parameters $K_p=0.2$, $K_i=0.5$, $K_d=0.03$ are set by optimization with above mentioned settings. Obtained phase margin is $\phi_m=60.1^0$. Later the gains are fixed and exponents are set to $\lambda=\mu=0.5$ and by enabling strict option the process is then continued. As a result, the exponents are obtained as $\mu=0.4$ and $\lambda=0.6$. By substituting the values, the transfer function of ACHBMLI given in (10) becomes:

$$G_v(s)=\frac{360}{2*10^{-8}s^2+8*10^{-5}s+1} \tag{15}$$

Transfer function of open loop system is given in (16). FO-PID Controller transfer function is given in (17). Overall system transfer function including controller is given in (18)

$$A(s)=\frac{1}{2*10^{-8}s^2+8*10^{-5}s+1} \tag{16}$$

$$C_{SL}(s)=\frac{0.03s^{1.05}+0.5s^{0.6}+0.5}{s^{0.6}} \tag{17}$$

$$Q(s)=\frac{0.03s^{1.05}+0.5s^{0.6}+0.5}{2*10^{-8}s^{2.6}+8*10^{-5}s^{1.6}+0.03s^{1.0}+1.5s^{0.6}+0.5} \tag{18}$$

Figure 4 and Figure 5 presents the bode plots for the open loop and closed system with and without controller. From the plot it is observed that the requirements specified in Table 2 were achieved.

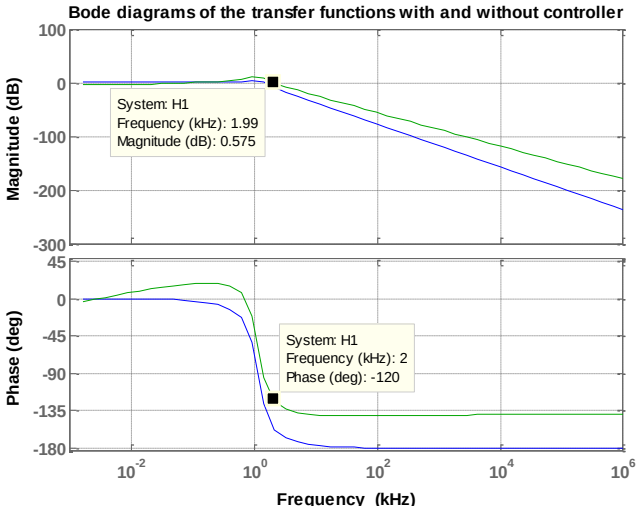


Figure 4. Bode plots of open loop transfer function

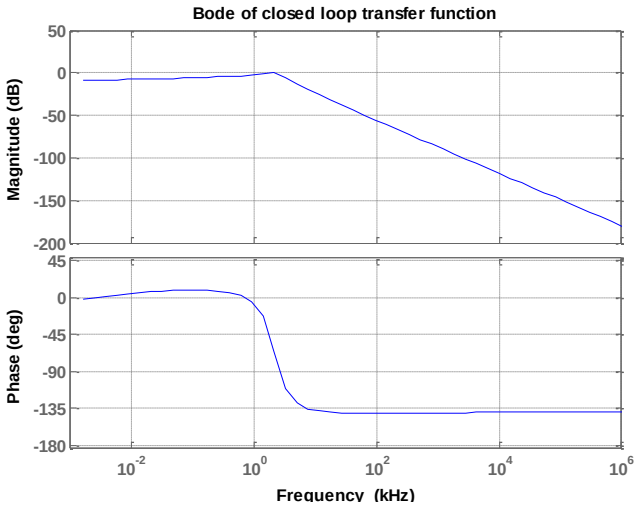


Figure 5. Bode plots of closed loop transfer function

4. RESULTS AND DISCUSSION

By using various level shifted modulating techniques the Asymmetrical CHBMLI with closed loop fractional order PID controller can be simulated using MATLAB. The parameters used for simulation are given in Table 3. The output voltage of inverter reduces due to addition of 50 ohm load resistance to the existing load resistance of 100 ohm at 2.5 sec. Table 4 gives the variations of load voltage under open loop with different modulation index. The variations of load voltage with different controllers are given Table 5. Total harmonic distortion (THD) of yield voltage of ACHBMLI for different modulation index and level shifted techniques with open loop and closed loop IO-PID and FO-PID controllers are shown in Table 6 and Table 7.

Table 3. Parameters of seven level ACHBMLI

Quantity	Value
Frequency of modulating wave	50 Hz
Carrier Wave frequency	3KHz
Module voltages	120V&240V
Load Resistance	R=100ohm to 33.33 ohm

Table 4. Output voltage (R.M.S) of ACHBMLI under open loop

m_a	TIME	ACHBMLI		
		PD	POD	APOD
0.8	t=0-2.5s	171.2V	170.2V	170.8V
	t=2.5-5s	168.8V	168.4V	168V
1	t=0-2.5s	212.5V	212.2V	212.2V
	t=2.5-5s	210.7V	210.5V	210V

Table 5. Comparison of output voltage (R.M.S) of ACHBMLI with different controllers

IO-PID controller			FO-PID controller		
PD	POD	APOD	PD	POD	APOD
228.9 V	228.5 V	228.7 V	229.9 V	229.5 V	229.2 V

Table 6. Voltage THD values for different m_a(open loop)

m_a	Asymmetrical CHBMLI		
	PD	POD	APOD
0.8	18.09%	18.21%	18.24%
1	12.17%	12.17%	12.25%

Table 7. Comparison of output voltage THD values with different controllers

IO-PID controller			FO-PID controller		
PD	POD	APOD	PD	POD	APOD
10.72%	11.38%	11.45%	6.32%	6.38%	6.45%

From above results it can be observed that the R.M.S value yield voltage increases and THD decrease as the modulation index increases. From Table 7 it can be observed that THD is less by providing closed loop with FO-PID controller compared to IO-PID controller. The different simulation waveforms obtained using PD-PWM for ACHBMLI were given in Figures 6 to 10. Figure 6 represented the voltage waveform obtained from the seven levels Asymmetrical CHBMLI circuit. The rms voltage of the output of

the inverter for two different modulation index values is given in Figure 7 Here the load variation is applied at t=2.5 seconds. It is found that there is huge variation in the rms values of the output voltage due to the open loop configuration. Figure 8 shows the rms value of the ACHBMLI under closed loop configuration with IO-PID and FO-PID controller. Even when there is a load change at t=2.5 sec the rms value of the output remains constant. Figure 9 shows the THD plots for the inverter in open loop configurations with modulation index (m_a) 0.8. Figure 10 shows the THD value plot for the inverter in closed loop configurations with IO-PID and FO-PID controller.

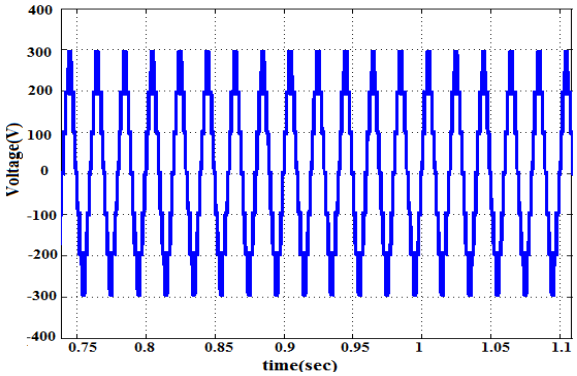


Figure 6. Output voltage of ACHBMLI

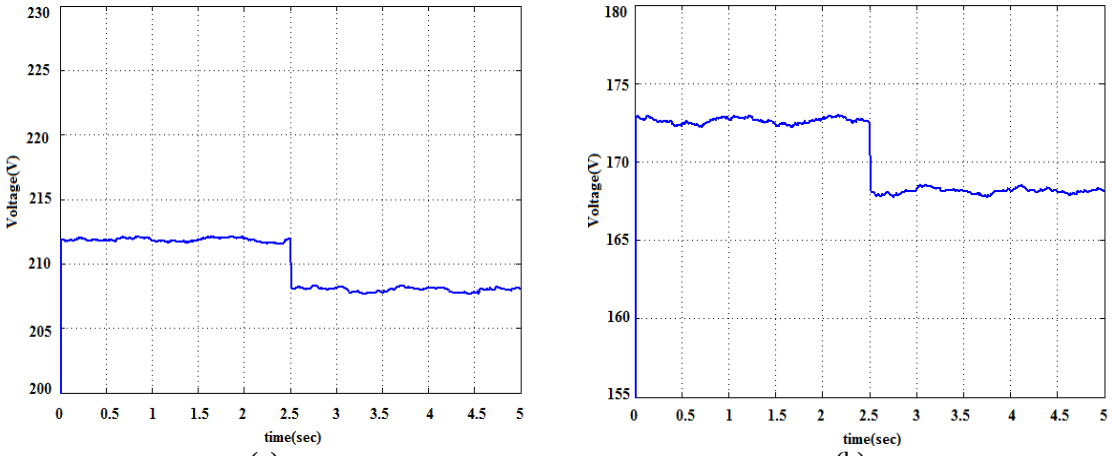


Figure 7. R.M.S. output voltage with, (a) m_a=1, (b) m_a=0.8

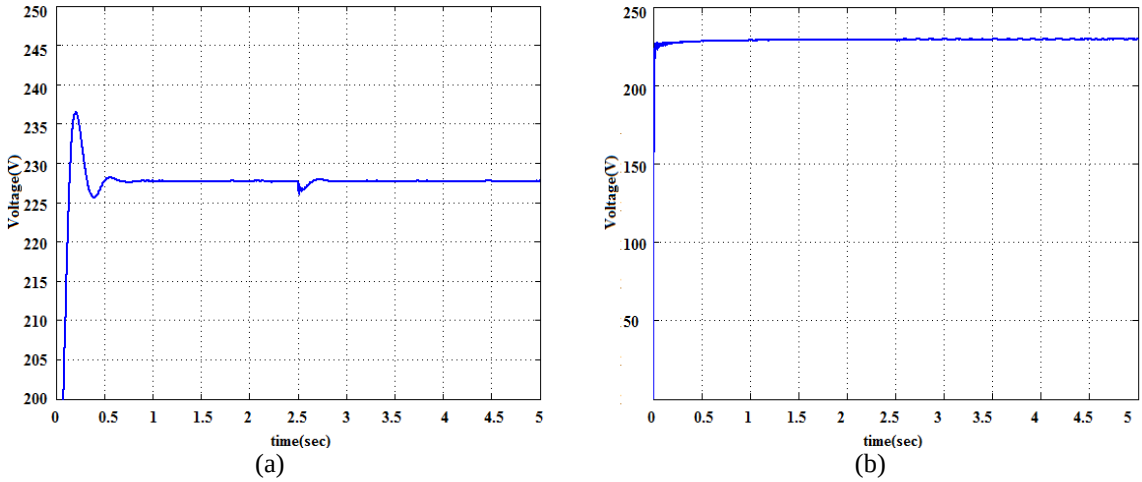


Figure 8. Output voltage of inverter with, (a) IO-PID controller, (b)FO-PID controller

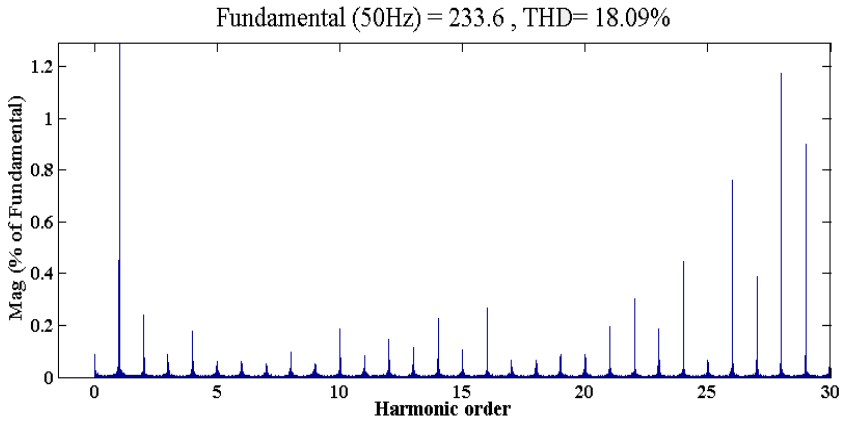
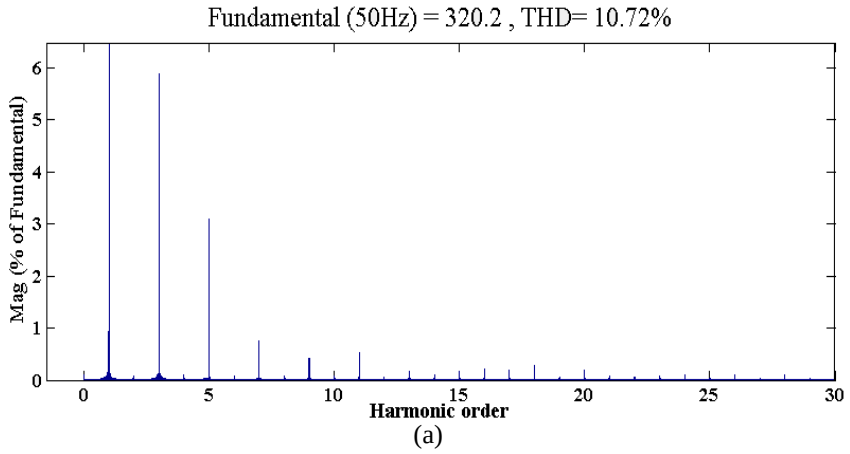
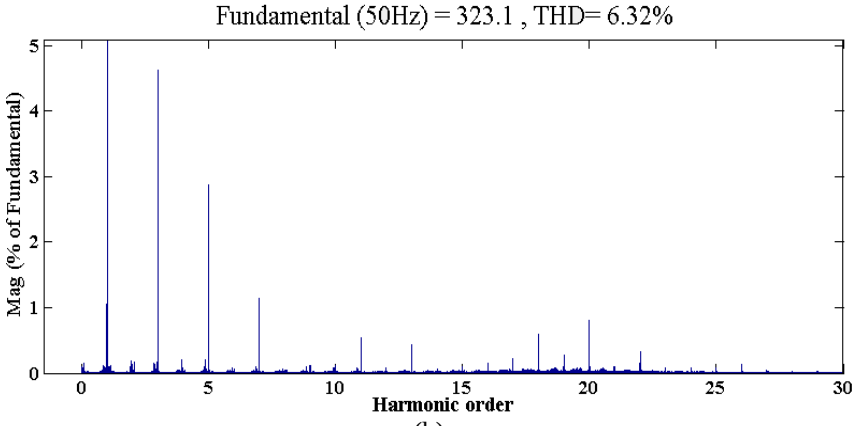


Figure 9. THD of output with m_a=0.8



(a)



(b)

Figure 10. THD with, (a) IO-PID, (b) FO-PID

5. CONCLUSION

This paper proposed a closed loop FO-PID controller design with the help of small signal model of ACHBMLI to control its output voltage.FO-PID provides better control performance for the system due to its more tuning parameters compared with Integer order PID controller. The simulation results indicate that the output voltage of the asymmetrical CHBMLI can be maintained constant and close to the reference voltage. The closed loop scheme also provides reduction in the harmonic distortion of output voltage of the inverter. This paper also compares different level shifted PWM techniques and from the results it was concluded that phase disposition technique yields better results compared to other level shifted techniques.

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REFERENCES

[1] E. H. Aboadla, S. Khan, M. H. Habaebi, T. S. Gunawan, B. A. Hamida, M. Yaacob, and A. Aboadla, "A novel optimization harmonic elimination technique for cascaded multilevel inverter," *Bulletin of Electrical Engineering and Informatics*, vol. 8, no. 2, pp. 405-413, Jun 2019.

[2] A. Ahmed, M. S. Manoharan and J. Park, "An efficient single-sourced asymmetrical cascaded multilevel inverter with reduced leakage current suitable for single-stage PV systems," *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 211-220, March 2019.

[3] P. Sochor and H. Akagi, "Theoretical and experimental comparison between phase-shifted PWM and level-shifted PWM in a modular multilevel SDBC inverter for utility-scale photovoltaic applications," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4695-4707, Sept.-Oct. 2017.

[4] C. R. Balamurugan and K.Vijayalakshmi, "Comparative analysis of various z-source based five level cascaded H-bridge multilevel inverter," *Bulletin of Electrical Engineering and Informatics*, vol. 7, no. 1, pp.1-14, Mar 2018.

[5] A. Ajami, M. R. J. Oskuee, M. T. Khosroshahi, and A Mokhberdoran, "cascade-multi-cell multilevel converter with reduced number of switches," *IET Power Electron.*, vol. 7, no. 3, pp. 552-558, Mar 2014.

[6] A. Ramesh, O. Chandra Sekhar, and M. Siva Kumar, "A novel three phase multilevel inverter with single DC link for induction motor drive applications," *International Journal of Electrical and Computer Engineering*, vol. 8, no. 2, pp. 763-770, Apr 2018.

[7] M. Khanfara, R. El Bachtiri, M. Boussetta, and K. El Hammoumi, "A multicarrier PWM technique for five level inverter connected to the grid," ," *International Journal of Power Electronics and Drive System*, vol. 9, no. 4, pp. 1774-1783, 2018.

[8] I. Colaka, E. Kabalcib, and R Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol. 52, no. 2, pp. 1114-1128, Feb 2011.

[9] S. Rathore and M. K. K. Bhardwaj, "Simulation of cascaded H-bridge multilevel inverter using PD, POD, APOD techniques," *Electrical & Computer Engineering: An International Journal (ECIJ)*, vol. 4, no. 3, pp. 27-41, 2015.

[10] H. Li, Y. Luo and Y. Chen, "A fractional order proportional and derivative (FOPD) motion controller: tuning rule and experiments," *IEEE Transactions on Control Systems Technology*, vol. 18, no. 2, pp. 516-520, March 2010.

[11] H. Ren, J. Fan and O. Kaynak, "Optimal design of a fractional-order proportional-integer-differential controller for a pneumatic position servo system," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6220-6229, 2019.

[12] T. Aleksei, P. Eduard and B. Juri, "A flexible MATLAB tool for optimal fractional-order PID controller design subject to specifications," *Proceedings of the 31st Chinese Control Conference*, Hefei, pp. 4698-4703, 2012.

[13] I. Birs, C. Muresan, I. Nascu and C. Ionescu, "A survey of recent advances in fractional order control for time delay systems," *IEEE Access*, vol. 7, pp. 30951-30965, 2019.

[14] T. D. C. Busarello, A. Mortezaei, H. K. M. Paredes, A. Al-Durra, J. A. Pomilio, and M. G. Simões, "Simplified small-signal model for output voltage control of asymmetric cascaded H-bridge multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3509-3519, April 2018.

[15] T. D. C. Busarello, A. L. de Sousa Marcondes Reuter, A. Péres, and M. G. Simões, "Understanding the staircase modulation strategy and its application in both isolated and grid-connected asymmetric cascaded H-bridge multilevel inverters," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5371-5382, Sept.-Oct. 2019.

[16] A. F. de S. Silva, S. P. Pimentel, E. G. Marra, and B. P. de Alvarenga, "Small-signal modeling of the single-phase asymmetrical cascaded multilevel inverter," *IEEE 38th Int. Conf. on Electr. and Nanotechnology*, pp. 686-691, 2018.

[17] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[18] C. Boonmee and Y. Kumsuwan, "A phase-shifted carrier-based PWM technique for cascaded h-bridge inverters application in standalone PV system," *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, pp. LS8c.3-1-LS8c.3-4, 2012.

[19] E. Babaei, "Optimal Topologies for Cascaded Sub-Multilevel Converters," Journal of Power Electronics, vol. 10, no. 3, pp. 251-261, May 2010.

[20] T. Sudha, "Comparison between cascaded multilevel inverter and reduced switch multilevel inverter," *International Journal for Research in Applied Science & Engineering Technology*, vol. 4, no.V, pp. 500-510, May 2016.

[21] J. Joseph and Aryaprakash, "Cascaded multilevel inverter with multicarrier PWM techniques," *International Journal of Engineering Science & Advanced Technology*, vol. 4, no. 5, pp. 437-442, 2014.

[22] R. Palanisamy, K. Vijayakumar, and D. Selvabharathi, "MSPWM based implementation of novel 5-level inverter with photovoltaic system," *International Journal of Power Electronics and Drive Systems*, vol. 8, no. 4, pp. 1494-1502, 2017.

[23] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *IET Pow. Elect.*, vol. 3, no. 5, pp. 702-715, 2010.

[24] A. J. Calderóna, B. M. Vinagrea, and V. Feliub, "Fractional order control strategies for power electronic buck converters," *Signal Process*, vol. 86, no. 10, pp. 2803-2819, 2006.

[25] A. Tepljakov, E. Petlenkov, and J. Belikov, "FOMCOM: A MATLAB toolbox for fractional-order system identification and control," *Int. Journal of Microelectronics and Computer Science*, vol. 2, no. 2, pp. 51-62, 2011.

BIOGRAPHIES OF AUTHORS

V.Anil Kumar wasborn in India on July 22, 1981. He received his M,E degree in Power Electronics & Drives from SreeSastha Institute of Engineering & Technology, Affiliated to Anna University, Chennai.Currently he is doing Ph,D in Pondicherry Engineering College, Pondicherry.

Dr. M. Arounassalame received the B.Tech. degree from Pondicherry University, India in 1993 and M.Tech. degree from University of Calicut, India in 1998. He received the Ph.D. degree in systems and control engineering from IIT Bombay, India in 2009. Presently, he is working as Associate professor at the Department of Electrical and Electronics Engineering, Pondicherry Engineering College, India.