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Analysis of analog and RF behaviors in junctionless double gate vertical MOSFET

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ABSTRACT

The prime obstacle in continuing the transistor's scaling is to maintain ultra-shallow source/drain (S/D) junctions with high doping concentration gradient, which definitely demands an advanced and complicated S/D and channel engineering. Junctionless transistor configuration has been found to be an alternative device structure in which the junction and doping gradients could be totally eliminated, thus simplifying the fabrication process. In this paper, a process simulation has been performed to study the impact of junctionless configuration on the analog and RF behaviors of double-gate vertical MOSFET. The result proves that the performance of n-channel junctionless double-gate vertical MOSFET (n-JLDGVM) is slightly better than the junction double-gate vertical MOSFET (n-JDGVM). Junctionless device exhibits better analog behaviors as the transconductance (gm) is increased by approximately 4%. In term of RF behaviors, the junctionless device exhibits 3.4% and 7% higher cut-off frequency (fT) and gain band-width product (GBW) respectively over the junction device.

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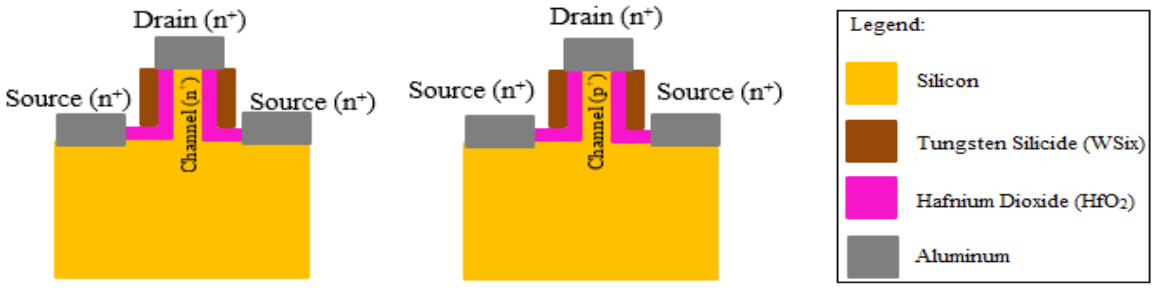
1. INTRODUCTION

The utilization of low power and high frequency based devices are very crucial for future electronic applications. Miniaturization in transistor's size with improvement in analog and RF performances is a vital goal of the microelectronics community. For realizing this goal, a number of device engineering methods such as source/drain engineering, multi-gate technology, dual material gate (DMG) technology, channel engineering, gate stack (GS) engineering and junctionless configuration have been carried out for decades [1–8]. According to International Technology Roadmap for Semiconductors 2013 (ITRS 2013) report [9], a precisely controlled process flow for the fabrication of transistors is becoming extremely complicated for deep sub-micron devices. As the transistor's size shrinks drastically towards sub-nanometer regime, the threshold voltage (VTH) would be rolled-off along with the decreasing channel length (Lch), which eventually deteriorating the overall performance due to short channel effects (SCE) [10]. The most difficult challenge in transistor's miniaturization is to form ultra-shallow source/drain (S/D) junctions with high doping gradient which requires advanced source/drain and channel engineering processes [11, 12]. For that reason, a lot of alternative device structures have emerged for realizing the Moore's law prediction without degrading the transistor performances.

Recently, the junctionless transistor configuration has received a lot of attention in producing the ultra-small, low power and high frequency transistor due to its simplified fabrication process [6, 8, 13–16]. Instead of having the intricate source/drain and channel engineering processes, the junctions of the transistor can be completely removed by doping the source/drain and channel regions with similar polarity dopant, either n-type (for n-channel transistor) or p-type (for p-channel transistor) dopant. The junctionless-mode configuration could avoid the adversity of forming the intricate junctions with high doping gradient, especially for short channel devices. The analog and RF behaviors in junctionless transistors are very important to be properly investigated, especially for system on chip (SoC) and system in package (SiP) applications [11, 17–19]. Thus, this paper emphasizes on the performance analysis of analog and RF behaviors of n-channel junctionless double-gate vertical MOSFET (JLDGVM) and n-channel junction double-gate vertical MOSFET (JDGVM). The presented work in this paper is organized as follows: Section 2 briefly describes the device simulation of both JLDGVM and JDGVM and the process flow using Silvaco simulator. Section 3 discusses the comparative analysis of the analog and RF behaviors between n-JLDGVM and n-JDGVM in term of transconductance (gm), transconductance generation factor (TGF), output conductance (gd), early voltage (VEA), gate-to-source capacitance (Cgs), gate-to-drain (Cgd), parasitic capacitance (Cgg), intrinsic gate delay (τint), cut-off frequency (FT) and Gain Band-Width product (GBW). Finally, the conclusions and future work are presented in section 4.

2. DEVICE SIMULATION

The devices are designed based on high-k material (hafnium dioxide) as gate stack and extensive investigation is conducted by taking junctionless and junction configuration to verify the effects on various analog and RF behaviors. The distinctive different between junctionless and junction configuration of double-gate vertical MOSFET is their opposite channel type as depicted in Figure 1. The channel region for n-JLDGVM is heavily doped with the similar polarity as source/drain doping in order to form N- N+- N type. In contrast, the channel region for n-JDGVM is doped with the opposite polarity as source/drain doping to form N-P-N type.



(a) (b)

Figure 1. 2D structure of n-channel double-gate vertical MOSFETs, (a) Junctionless (n-JLDGVM), (b) Junction (n-JDGVM)

Extensive device simulation is performed via Silvaco Atlas for extracting the DC and AC characteristics of n-JLDGVM and JDGVM devices. The device simulation is conducted based on the current continuity and drift diffusion models in order to compute the current-voltage characteristics. Besides that, the mobility model is also included for considering the scattering processes such as lattice vibration (phonons), impurity ions, surfaces, and other material imperfections. The impact of these scattering processes would lead to low carrier mobility since they involve in both current continuity and drift-diffusion models [20]. For this case, the Lombardi CVT model is opted to be employed to perform accurate simulation of non-planar MOSFET like JLDGVM and JDGVM devices.

3. RESULTS AND DISCUSSION

In this section, the simulation results and discussion are critically described for both n-JLDGVM and n-JDGVM devices. For the purpose of performance analysis of analog and RF behaviors in JLDGVM

and JDGVM devices, the VTH values of both devices were fixed at 0.2 V. The other DC characteristics are normalized to the fixed VTH value for unbiased performance evaluation. The DC analysis is an initial step for the further evaluation of analog and RF behaviors in both devices. The analog and RF behaviors for both devices are discussed in the following sub-sections.

3.1. Analog behaviors

Analog behaviors such as transconductance (gm), transconductance generation factor (TGF), drain conductance (gd) and early voltage (VEA) are presented and discussed here for analog performance point of view. The transconductance (gm) is an important figure of merit that implies how effective a transistor converts a voltage to a current. It is mainly employed for measuring the amplifier's gain. On the other hand, the transconductance generation factor (TGF) is also a significant figure of merit that implies how efficient a transistor converts DC power into AC frequency and gain. Figures 2 and 3 present the plot for gm and TGF respectively as a function of gate voltage (VG). The n-JLDGVM device demonstrates approximately 4% higher tranconductance (gm) than the JDGVM device. Below the gate voltage (VG) of ~ 0.6V, the gm for both devices linearly increases as the VG increases. After VG ~ 0.6V, the gm for both devices begins to saturate until its reach maximum gate bias. It is observed that the maximum gm at VG=1 V for n-JLDGVM device is approximately 4% higher than the n-JDGVM device. Due to bulk phenomenon in junctionless configuration, the gm is slightly increased as it is approaching the maximum gate voltage. The improved gm value in junctionless configuration agreed with previous works conducted [16]. A higher gm of the n-JLDGVM device indicates that the conducting channel possesses higher transport efficiency which is suitable for analog based applications. In term of TGF, the n-JLDGVM device demonstrates approximately 20% higher TGF compared to JDGVM device. The slight improvement in TGF is in agreement with the results obtained by previous researchers [21, 22]. The gm/ID ratio is mainly influenced by the pillar/body factor of the devices in weak inversion region. However, the gm/ID ratio for n-JDGVM is observed to be slightly decreased due to strong inversion in the channel region that causes a decrease in electron mobility at higher doping concentration.

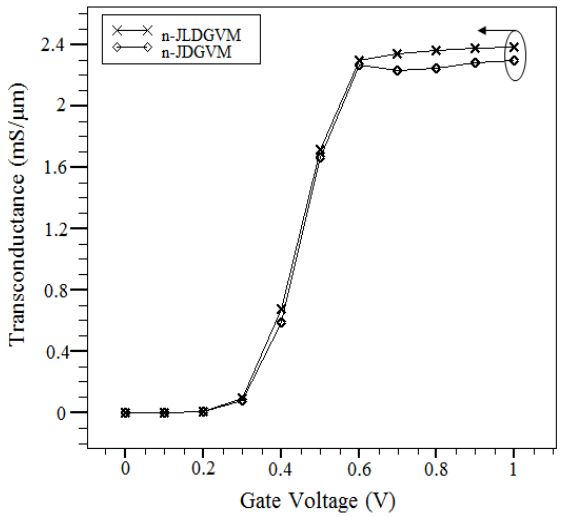


Figure 2. Transconductance (gm) as a function of gate voltage

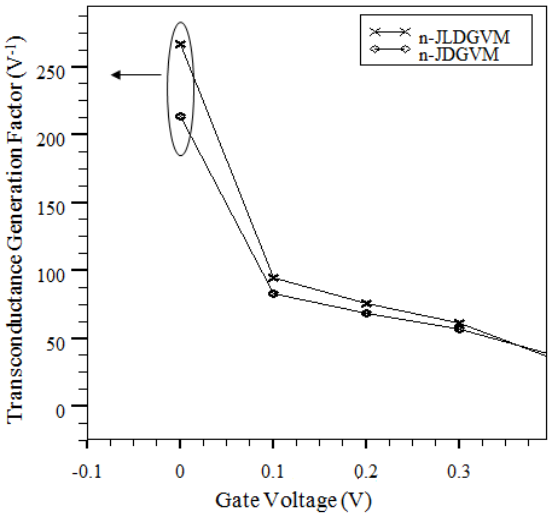


Figure 3. TGF as a function of gate voltage

The drain conductance (gd) is also an important analog characteristic that decides a transistor's performance in analog based applications. The ultrathin pillar feature in both n-JLDGVM and n-JDGVM devices are very crucial in forming a fully depleted channel that could reduce the impact ionization effects. The impact ionization effects such as kink effect and parasitic bipolar action, normally experienced in most of bulk transistors would subsequently lead to a much higher gd. The value of gd is very crucial in determining the drain current (ID) to drain conductance (gd) ratio, also called as early voltage (VEA). The VEA is not a constant value, but depends upon the channel length, inversion level and also the drain voltage (VD). Figures 4 and 5 show the plot of drain conductance (gd) and the early voltage (VEA) respectively at VG=0.5V as a function of VD. The n-JLDGVM device carries higher drain current and thus results in higher drain conductance than the n-JDGVM device.

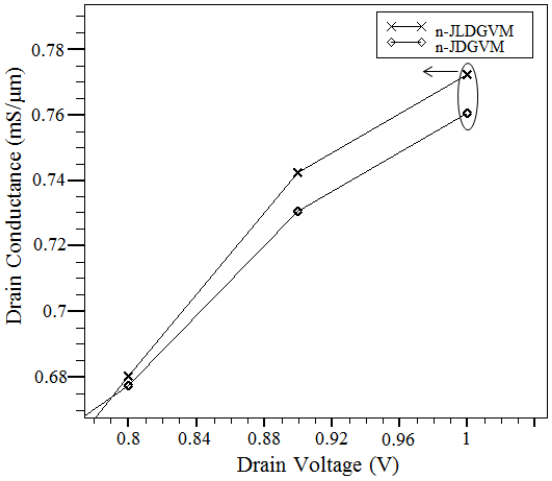


Figure 4. Drain conductance (gd) as a function of drain voltage

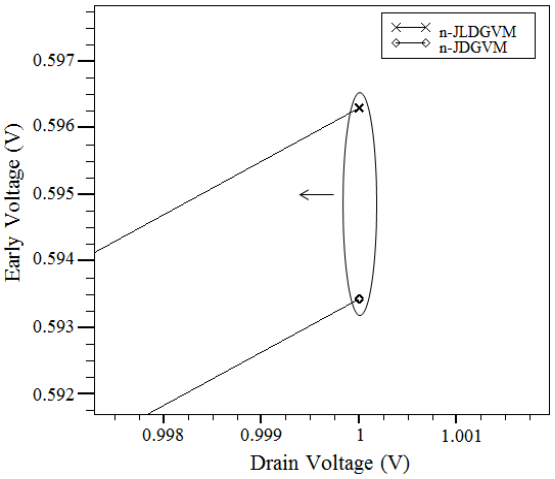


Figure 5. Early voltage (VEA) as a function of drain voltage

The n-JLDGVM device exhibits approximately 11% higher gd than n-JDGVM device. In most cases, the gd magnitude is strongly influenced by channel length modulation. In practical, CMOS analog circuits preferably need MOSFETs that exhibit low gd magnitude for attaining much higher gain. A slight improvement (0.5%) in VEA can be observed in case of n-JLDGVM device as compared to n-JDGVM, mainly due to short channel effects (SCE) suppression. The side gates have better control over the charge carriers in the junctionless mode which slightly mitigating the SCE. As a result, the value of early voltage in n-JLDGVM device slightly increases and the dependence of the drain current on the drain voltage is minimized. Evidence of improved VEA for junctionless configuration is also reported by [11, 16]. The intrinsic gain (AV) is another important figure of merit for benchmarking the analog performance of operational transconductance amplifiers. The AV for the devices can be calculated as:

$$A_V = \frac{g_m}{g_d} = \left(\frac{g_m}{I_D}\right) \times V_{EA}$$

The extracted and computed values of gm, TGF, gd, VEA and AV for n-JLDGVM and n-JDGVM devices are summarized in Table 1. It is observed that the n-JLDGVM device exhibits marginally 2% higher AV than n-JDGVM device. Higher AV is pretty much desired in analog designs because it implies how efficient a transistor could amplify the input signal when it is biased to operate in both active and saturation region of operation.

Table 1. Analog performances for JLDGVM and JDGVM

Device	g_m (mS/μm)	TGF (V^{-1})	g_d (mS/μm)	V_{EA} (V)	A_V (dB)
JLDGVM	2.39	267	0.772	0.596	9.8
JDGVM	2.30	214	0.761	0.593	9.6

3.2. RF behaviors

Several crucial RF behaviors of the device are extracted and computed. Initially, the extractions of Cgs and Cgd are carried out through small signal analysis after post-processing DC analysis. The values of capacitance between source and drain regions are measured by supplying a single AC frequency (f) of 1 MHz as the VG is swept from 0 V to 1 V with a step of 0.01 V. Figures 6 and 7 depict the plot of intrinsic capacitances (Cgs and Cgd) respectively as a function of VG at a fixed VD of 0.5 V. Based on the combined plot, the Cgs for n-JLDGVM device is observed to be approximately 3% higher than the n-JDGVM device. Furthermore, both devices show an almost linear increase in Cgs value as the gate voltage is shifted towards its maximum value (1 V). The difference of Cgs for both devices is less prominent as it does not contribute significant changes in output current when the gate is turned off and the time required for the output to turn off completely. On the other hand, the n-JLDGVM device exhibits approximately 3% lower Cgd compared to n-JDGVM device. Both devices exhibit an almost constant Cgd value as the gate voltage is shifted towards its maximum value (1V). The high Cgd is not desirable in RF and high frequency applications because it would delay the rise in drain current after the gate is turn on and the fall in drain current after the gate

is turned off. As consequence, the switching speed is greatly reduced by the increasing Cgd. The Cgg, also known as the parasitic gate capacitance is an important characteristic for determining the intrinsic gate delay of a transistor. Figure 8 shows plot for the Cgg as a function of VG at a constant VD of 0.5V. The n-JLDGVM device demonstrates a slight decrease in Cgg over the n-JDGVM device. A larger Cgg definitely would result in higher gate delay.

The intrinsic gate delay is used to indicate the frequency limit of RF circuits. The intrinsic gate delay of a transistor heavily depends on the parasitic gate capacitance (Cgg). A higher intrinsic gate delay would affect the propagation of majority carriers (electrons), especially in high frequency applications. Figure 9 shows the plot for the intrinsic gate delay (τint) as a function of drain voltage at a constant gate voltage of 0.5V. The n-JLDGVM device exhibits approximately 3% lower τint than n-JDGVM device at maximum drain voltage (1V). Both devices demonstrate a significant increase in τint before the drain current saturates. After the drain current for both devices saturates, their corresponding τint begin to decline tremendously. Another transistor's characteristic that is crucial for RF and high frequency application is known as cut-off frequency (fT). The fT is a figure of merit of a transistor to reflect both frequency response and gain. The fT represents a unity gain frequency of a transistor amplifier that is majorly driven by input and output RC constants. The value of intrinsic capacitances is a dominant factor that drives the frequency response since the value of gm predominantly governs the voltage gain. Besides that, it is also important to consider the gain-band-width product (GBW) of both devices for the purpose of high frequency transient analysis.

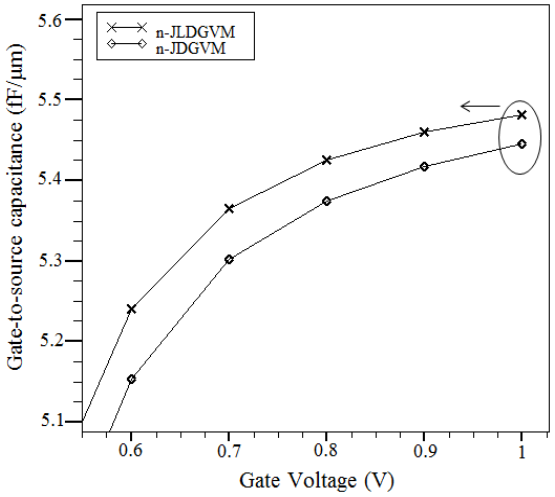


Figure 6. Cgs as a function of VG

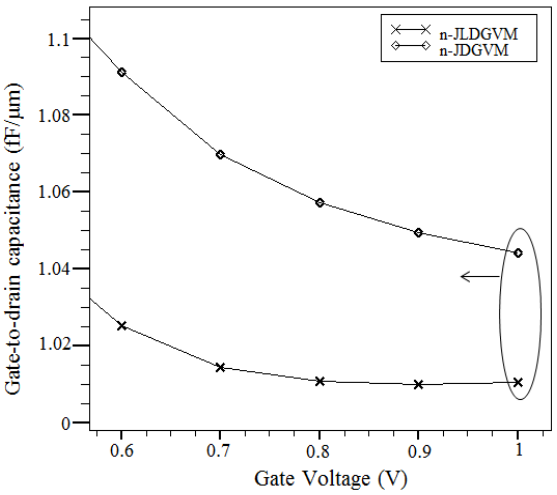


Figure 7. Cgd as a function of VG

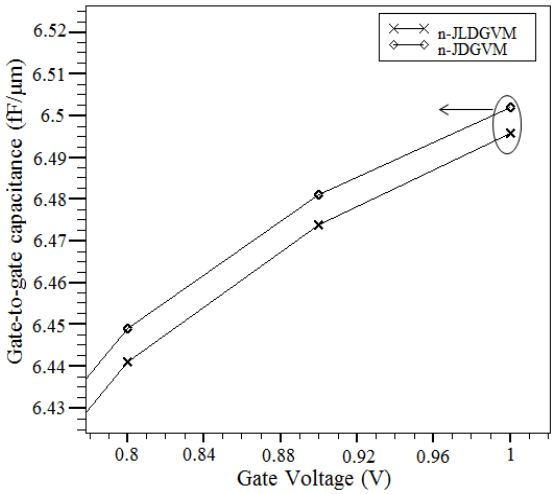


Figure 8. Cgg as a function of VG

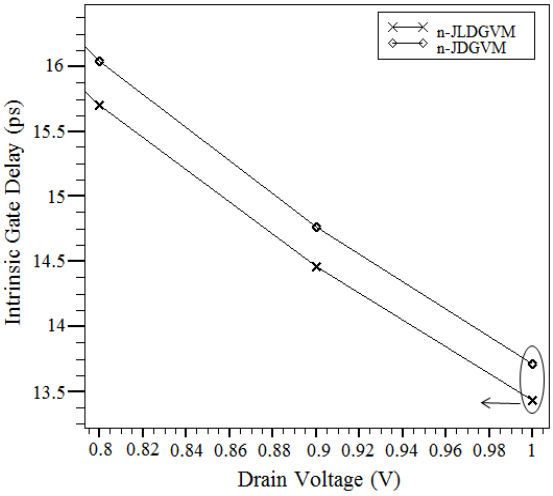


Figure 9. τ_{int} as a function of V_D

Figures 10 and 11 depict the plot of fT and GBW respectively for both devices as a function of gate voltage at a constant drain voltage of 0.5V. The n-JLDGVM device exhibits approximately 3.4% higher fT

compared to n-JDGVM device. The slight improvement in fT for n-JLDGVM device over the n-JDGVM device is due to junctionless configuration which alters the energy band structure of the conductive layer. As a result, the effective mass of electrons is slightly reduced, thus increasing its mobility. The variation of fT over the increasing gate voltage is mainly affected by the gm and the intrinsic capacitances. Hence, high gm and low intrinsic capacitances are significantly required in achieving better cut-off frequency (fT) for high speed RF applications. In term of GBW, the n-JLDGVM device shows 7% higher GBW than the n-JDGVM device. The minor improvement in GBW of n-JLDGVM device is mainly influenced by its higher gm and the lower Cgd than the n-JDGVM device. The high GBW is very desirable for circuit applications that require extremely high speed and low input bias current such as RF amplifiers [23]. The extracted and computed values of Cgs, Cgd, Cgg, τint, FT and GBW for n-JLDGVM and n-JDGVM devices are summarized in Table 2. Based on the obtained results, it can be concluded that the junctionless configuration does improve the overall device characteristics of double-gate vertical MOSFET, including the analog and RF behaviors. A slight improvement in ID, gm, TGF, gd, VEA, AV, Cgs, Cgd Cgg, τint, fT and GBW clearly indicate that the n-JLDGVM device can be a potential transistor configuration for future low power and high frequency analog and RF applications. However, the analog and RF behaviors for the n-JLDGVM device still could be further improved by optimizing the geometrical and process parameters. Thus, various optimization methods [24–30] could be applied to further enhance the DC and AC characteristics for analog and RF applications.

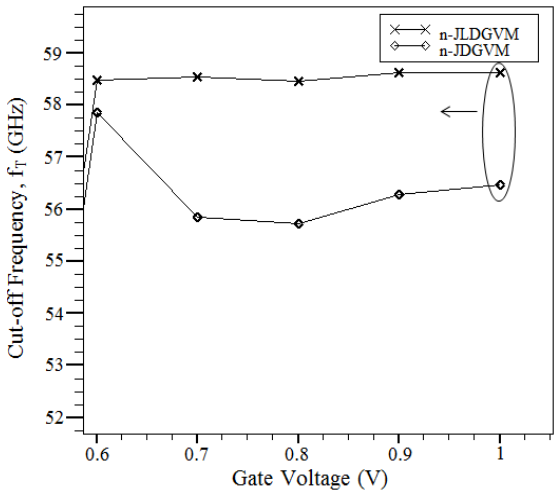


Figure 10. f_T as a function of V_G

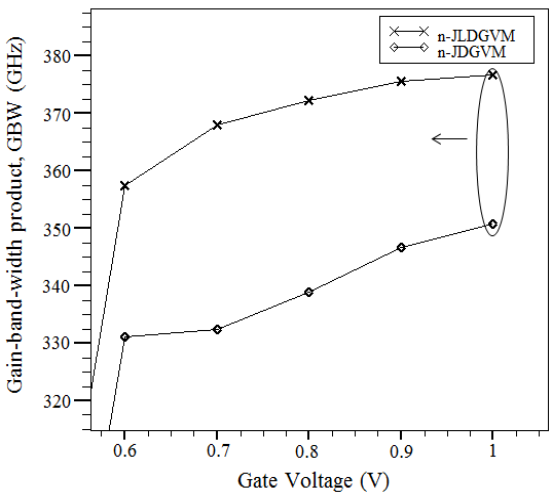


Figure 11. GBW as a function of VG

Table 2. RF performances for JLDGVM and JDGVM

Device	C_{gs} (fF/μm)	C_{gd} (fF/μm)	C_{gg} (fF/μm)	τ_{int} (ps)	f_T (GHz)	GBW (GHz)
JLDGVM	5.48	1.01	6.49	13.4	59	377
JDGVM	5.45	1.04	6.50	13.7	57	351

4. CONCLUSION

In summary, the DC, analog and RF behaviors of n-channel junctionless double-gate vertical MOSFET (n-JLDGVM) are investigated and compared with the n-channel junction double-gate vertical MOSFET (n-JDGVM). The device performance between n-JLDGVM and n-JDGVM are compared in term of gm, TGF, gd, VEA, AV, Cgs, Cgd Cgg, τint, fT and GBW. The results show that the junctionless device demonstrates slightly better analog behaviors over the junction device as the gm magnitude is increased by 4%. In term of RF behaviors, the junctionless device exhibits 3.4% and 7% higher fT and GBW respectively over the junction device. These show that n-JLDGVM device can be a potential transistor configuration for future low power and high frequency analog and RF applications. Furthermore, both analog and RF behaviors of the n-JLDGVM device could be possibly improved by optimizing geometrical and process parameters through statistical methods or predictive analysis.

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