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A 28 GHz high efficiency fully integrated 0.18 µm combined CMOS power amplifier using power divider technique for 5G millimeter-wave applications

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ABSTRACT

A 28 GHz power amplifier (PA) using CMOS 0.18 µm Silterra process technology for milimeter wave applications is reported. Maximizing the power added efficiency (PAE) and output power are achieved by optimize the circuit with power divider and cascade configuration. In addition, reverse body bias is also employed for realizing excellent PAE and power consumption. A three stage CMOS PA with power combiner is designed and simulated. The simulation results show that the proposed PA consumes 62.56 mW and power gain (S_{21}) of 8.08 dB is achieved at 28 GHz. The PA achieves saturated power (P_{sat}) of 12.62 dBm and maximum PAE of 23.74% with output 1-dB compression point (OP_{1dB}) 10.85 dBm. These results demonstrate the proposed power amplifier architecture is suitable for 5G applications.

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1. INTRODUCTION

In the midst of the pervasive growth of the fifth generation (5G) millimeter-wave technology, the design of millimeter-wave (mm-wave) systems become challenging as the demand of broadband data traffic increased [1]. Efficiency of the transceiver is required in mm-wave systems and the sub block of the transceiver which is power amplifiers play significant performance in transmitters due to extensive power consumption [2-4]. As CMOS technology offer low cost and high integration level for manufacturing volume, it does attract the design for transceiver system [5, 6]. As a result, many mm-wave CMOS power amplifiers have been implemented in [7]. However, high efficiency silicon power amplifier (PA) for mm-wave communications is challenging due to ingrained trade-off between break-down and speed in silicon [8]. For example, the cut-off frequency (f_T) and oscillation frequency (f_{MAX}) of the MOS transistor in 0.18 µm CMOS process are about 50 GHz and 55 GHz (pre-layout simulation results) which will restraint the power gain of the CMOS power amplifier [8, 9].

Low breakdown voltage and high substrate loss also interrupt the performance of power efficiency and output power [10, 11]. To demonstrate high PAE and low power consumption can be achieve simultaneously for a 28 GHz CMOS PA, in this work, we report a 28 GHz PA with excellent PAE, P_{sat}

and low power consumption properties using 0.18 µm Siltera process technology. The proposed PA comprises two 3 cascade stages combine using power divider to achieve high PAE. The paper is organized as follows, section 2 discuss on mm-wave challenge. Section 3 explains the detailed circuit design. The reverse body bias is used to achieve high efficiency. 3 cascade topology is applied to increase the output power PA. Finally, power combiner technique is proposed to improve the existing PAE of the cascade stage. Section 4 presents the simulation results of the PA and section 5 concludes this paper.

2. MM-WAVE CHALLENGE

As mobile data growth and the used of smart phone increased nowadays, it's create peculiar contest for wireless service provider to overcome a global bandwidth shortage [12]. Therefore, the mm-wave frequency spectrum is being explored to overcome this issue. Many researches experience a lot of challenges in implementing mm-wave power amplifiers. The existence of parasitic capacitance to ground from the transistor node significantly degrades power added efficiency (PAE) at mm-wave frequencies [13]. A proper impedance matching for the design is needed to cancel parasitic capacitors and consequently improves the PA's PAE [14].

The power gain trade-off due to transistor sizing that presents itself at mm-wave frequencies shows an upper limit on the maximum transistor size that can be achieved with reasonably high gain in a single transistor [13]. Moreover, the power gain output trade-off due to impedance matching makes it more challenging to achieve reasonable power gain from a single stage amplifier [15, 16].

At mm-wave frequency spectrum, it is harder to achieve high output power level due to the low supply voltage that accompanies smaller technology nodes [17]. Besides, the technology shrinks causing the gate oxide become thinner and breakdown voltage become lower hence limit to get better output power at receiving end of the system [15].

Energy consumption has recently become an important consideration for wireless communication protocols. The shrinking size of the transistor and increasing density of next-generation wireless devices imply reduced battery capacities [18]. Therefore, low power consumption is needed in the design to prolong the usage time and extend the battery life.

3. CIRCUIT DESIGN

The power amplifier is the last output stage in the transmitter architecture; it provides the power amplification of an input signal to an antenna and plays a critical part in determining entire power efficiency of a transmitter [19, 20]. Among various types of power amplifiers described in the previous chapter, a Class E power amplifier was designed in this research. In the power amplifier built with several stages, the most critical stage is the output stage that consumes most of the current [21]. Considering efficiency, output power, and bias current, the power amplifier provides sufficient gain while maintaining reasonably high efficiency [22-24].

This section shows how CMOS power amplifier is designed to obtain a high-performance power amplifier over the specification. The goal is to design and implement a CMOS power amplifier that can be integrated in mm-wave 5G applications. Selecting the power amplifier structure, the transistor size and the optimum load impedances for each stage are determined. Also, several key design parameters such as biasing circuit, stability, and cut off frequency also need to be considered in the early stage design. To design the proper input and output matching networks as well as to obtain high efficiency in the power amplifier, the conjugate matching and combiner methods are used. The design with reverse body bias and combiner are explain in the following sub-section.

3.1. Reverse bias technique

The schematic design of cascade power amplifier is shown in Figure 1. Cascade topology has been chosen to provide sufficient gain. To achieve the desired output power at the power amplifier output, the transistor width of M_1, M_2 and M_3 are optimize to be 48, 50 and 95 µm respectively. The first stage consist of reverse body bias to control the power consumption at first stage (P_{DC1}), to get the high efficiency and low power consumption. The output of the first stage PA is passed to the other stage through an inter-stage matching circuit formed by capacitors C_1 and C_2 which is designed and optimized to achieve maximum PAE and output power. The design with the three-stage of cascaded amplification is chosen to achieve the required gain. The output stage is designed to provide maximum output power while the first and second stages are designed for maximum gain.Power gain of the cascade system increase due to current and voltage gain increased by cascading the amplifier stage [25]. Therefore, the need for cascading is important to maintain the power gain.

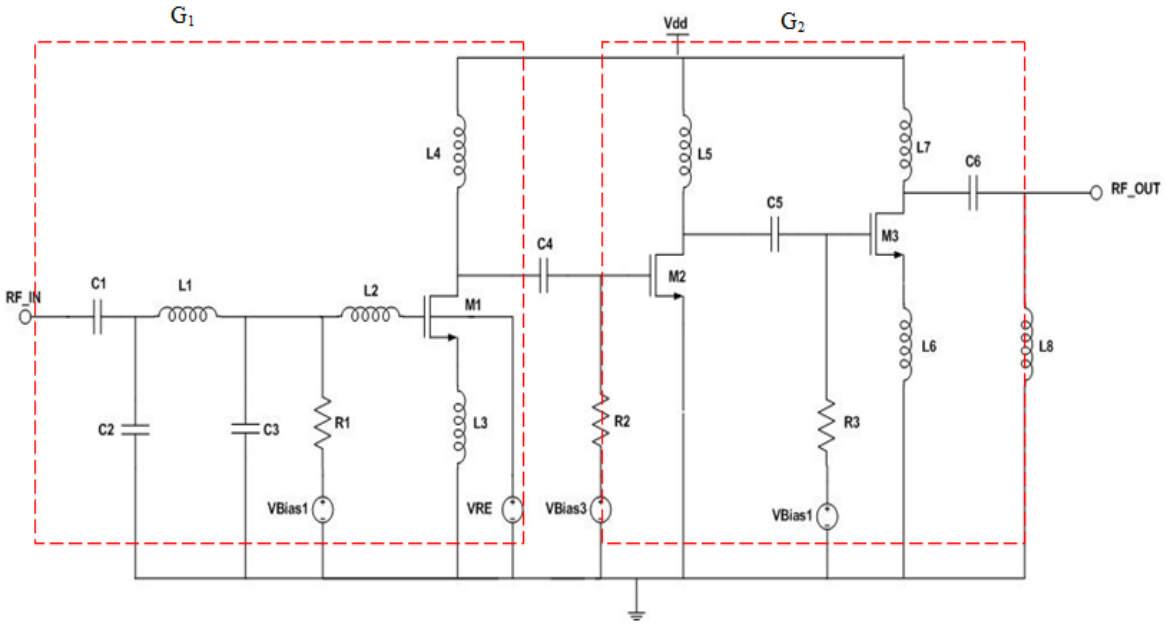

Figure 1. Schematic diagram of the three-stage CMOS PA with reverse bias. The drain current, I_d, in the saturation region, depends on the W/L ratio of transistor, gate bias voltage (V_{gs}) and threshold voltage (V_t)

$$I_d = k' \frac{W}{L}\left[(V_{gs} - V_t)V_{dsat} - \frac{V_{d,sat}^2}{2}\right] \quad (1)$$

where the threshold voltage define as ;

$$V_T = V_{TO} + \gamma(\sqrt{|-2\varphi_F + V_{SB}|} - \sqrt{|-2\varphi_F|}) \quad (2)$$

from (2), the source to bulk voltage (V_{SB}) play an important role to control the V_T. As V_{SB} decreased, V_T will be increased resulting lower I_d. As I_d lower, total power consumption of the device (P_{DC}) will be decreased, eventually it will drive to better efficiency of the circuit as power added efficiency (PAE) is depend on ;

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (3)$$

noted that for cascade topology, total efficiency is equivalent to;

$$\eta_{total} = \frac{\eta_2}{\left[\frac{P_{DC1}}{P_{DC2}} + 1\right]}\left[1 + \left(\frac{G_1 - 1}{G_1}\right)\left(\frac{1}{G_2 - 1}\right)\right] \quad (4)$$

where G_1 and G_2 are stage one and two respectively. Notice that, from (4) if the $P_{DC1}$is minimum and $G_2$is high, the efficiency of the PA will be increased. Therefore, to reduce the P_{DC1}, reverse bias technique at the input stage is applied while G_2 is set to be high by cascading the circuit.

3.2. Power combiner

Wilkinson power combining technique will be utilize in this design to obtain greater efficiency, the radio frequency signal is being divided into two paths using Wilkinson power divider and two RF

amplifiers are fed with the divided RF signal. The output stages of each amplifier are then combined with Wilkinson power combiner. At the output stage, the output power of the system will be high compared to single amplifier design. Linearity of the power amplifier also improve as the RF power increased. In this design, to achieve high output power, 2 power amplifiers are combined as shown in Figure 2 using Wilkinson power divider and combiner. A λ/4 transmission line is model using a lumped element pi equivalent network as shown in Figure 3. Using this equivalent circuit, two main power amplifiers from Figure 1 are combined as shown in Figure 4.

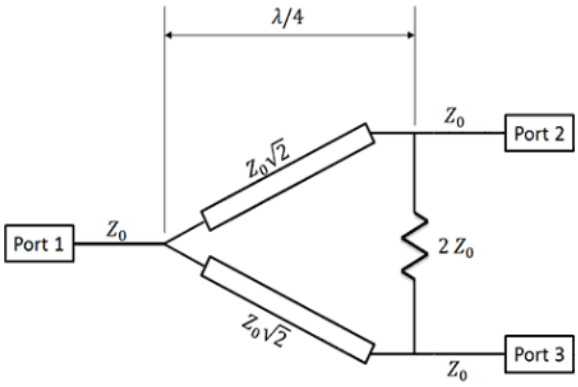

Figure 2. Microstrip patch wilkinson power divider

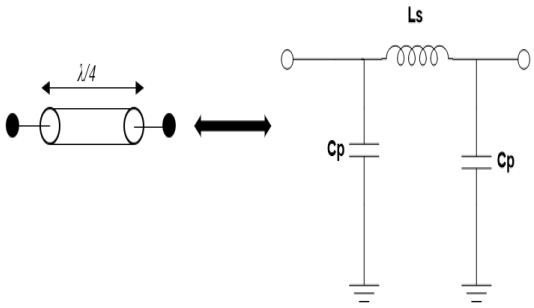

Figure 3. Lumped element Pi equivalent network

Lumped element network is derive as follows;

$$L_s = \frac{\sqrt{2}}{2\pi f_o} Z_o \tag{5}$$

$$C_p = \frac{1}{2\pi f_o Z_o} \tag{6}$$

where Z_o is 50 Ω and f_o is target frequency.

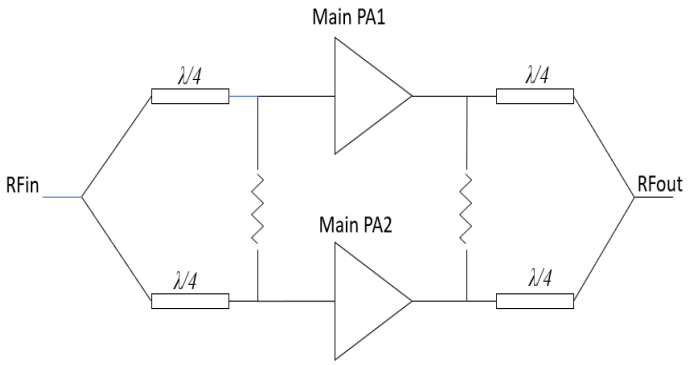

Figure 4. Proposed schematic design

4. SIMULATION RESULT AND DISCUSSION

S-parameter simulation results are shown in Figures 5, 6 and 7. The power amplifier provides a simulated peak S_{21} of 8.08 dB at 28 GHz. The S_{21} 3-dB bandwidth is 6.99 GHz centered around 26 GHz as shown in Figure 5. As the input is matched to 50 Ω impedance, it provide a peak simulated S_{11} of -12 dB at 26 GHz. The S_{11} 10-dB bandwidth is 3.1 GHz ranging from 24.4 GHz to 27.5 GHz as shown in Figure 6.

As the output is matched to 50 Ω impedance, it provides peak simulated S_{22} of -27.2 dB at 28.37 GHz. The S_{22} 10-dB bandwidth is 9.58 GHz ranging from 21.76 GHz to 31.34 GHz as shown in Figure 7.

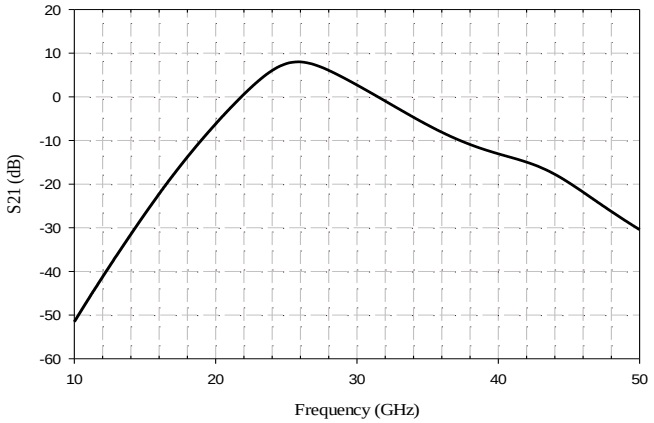

Figure 5. Simulated S_{21} versus frequency at 28 GHz

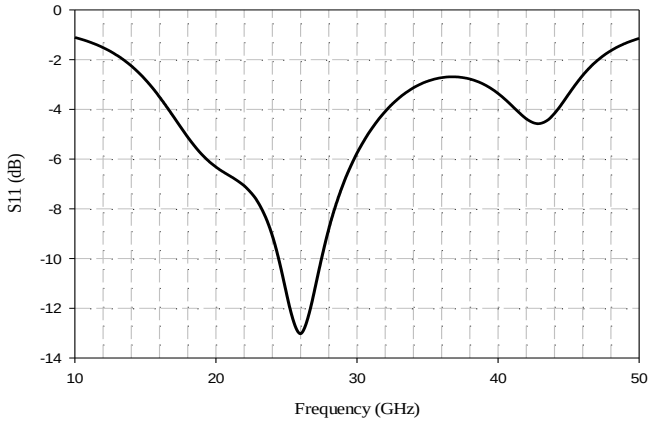

Figure 6. Simulated S_{11} versus frequency at 28 GHz

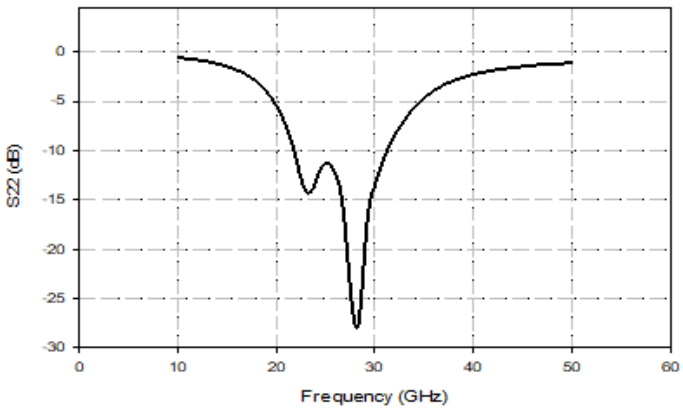

Figure 7. Simulated S_{22} versus frequency at 28 GHz

Power simulation results are shown in Figures 8 and 9 The power amplifier delivers a 1 dB compression and saturated output powers of +10.85 dBm and+12.62 dBm respectively as shown in Figure 8. The power gain obtained for design PA is 6.67 dB and the peak simulated power added efficiency is 23.74% as shown in Figure 9. The amplifier consumes only 62.56 mW from 1.9 V power supply. Comparison of CMOS PA performances as shown in Table 1.

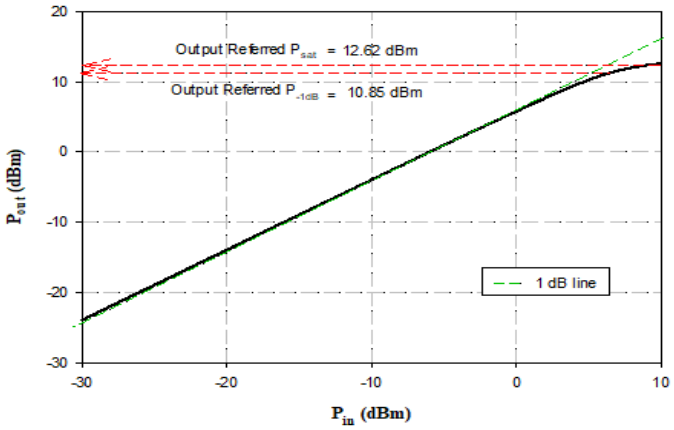

Figure 8. Simulated P_{1dB} of the PA at 28 GHz

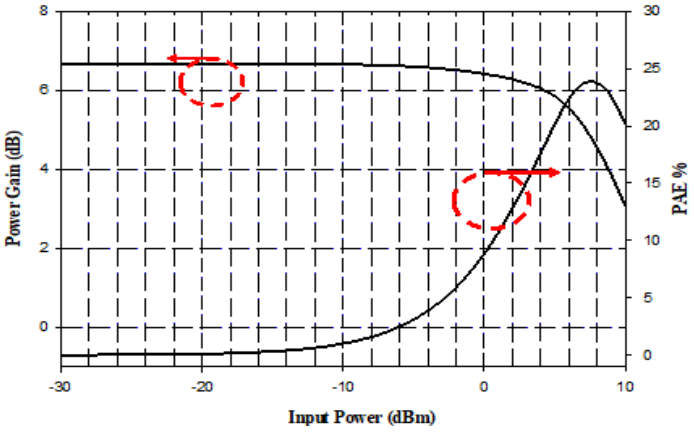

Figure 9. Simulated power gain & PAE of the PA at 28 GHz

Table 1. Comparison of CMOS PA performances

Parameter	[13]	[17]	[15]	[19]	[20]	This Work
Technology (µm)	0.18	0.25	0.18	0.18	0.25	0.18
Frequency (GHz)	26	27	23	23	23-30	28
PAE %	13.2	13	14.6	14.2	15	23.74
Gain (dB)	15.2	20.7	23	13.9	14	6.67
Psat (dBm)	19.5	31	15.7	15.7	16.8	12.62
S_{22}(dB)	-7	-5	-15	-15	-7	-27.2

5. CONCLUSION

This work addresses the requirements, and challenge of realizing an efficient mm-Wave PA in standard CMOS technology for 5G application. A combined 3 stage cascade with reverse bias topology at 28 GHz CMOS PA is presented. The amplifier is implemented in a standard CMOS 0.18 µm process. The proposed topology employed cascade structure with power combiner and divider to obtain high PAE with reverse body bias at input stage to achieve better efficiency. Table 1 show the comparison with other's researcher. The proposed design exhibit better efficiency and output return loss compare to other's researcher. The simulation results show that the proposed PA is able to deliver 10.95 dBm of output power to

a 50 Ω load with PAE of 23.74% at power consumption of 62.56 mW using a 1.9 V voltage. The proposed PA can be used for future 5G communications.

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Assoc. Prof. Dr Tun Zainal Azni Zulkifli received the B.Sc., M.Sc., and D.Sc. degrees in electrical engineering from shington University, St. Louis, MO, USA, in 1995, 1998, and 2002, respectively. Prior to 1995, he spent two years as a Product Engineerwith NEC Semiconductors (M) Sdn Bhd, where he was responsible for various products such as regulators and amplifiers. He completed and co-lead MP-45G linetransfer from NEC Fukui to Malaysia in 1994. From 2002 to 2014, he was with Universiti Sains Malaysia leading RFIC Group developing various wireless transceivers for UWB, RFID, and WCDMA specifically. He was also involved in pursuing some data converters implementation and FFT development. In 2005, he co-designed successfully active RFID RF Front End specifically LNA, mixers, and bandgap reference for Jaalaa Inc., Lake Forest, CA, USA. Since 2014, he has been with UniversitiTeknologi PETRONAS, where he has been leading the RFIC Group. To date, he has over 79 technical publications and successfully supervised four Ph.D. and seven M.Sc. candidates.