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# 0.18µm-CMOS Rectifier with Boost-converter and Duty-cycle-control for Energy Harvesting

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**ABSTRACT**

Existing works on battery-less of energy harvesting systems often assume as a high efficiency of rectifier circuit for power management system. In practice, rectifier circuit often varies with output power and circuit complexity. In this paper, based on a review of existing rectifier circuits for the energy harvesters in the literature, an integrated rectifier with boost converter for output power enhancement and complexity reduction of power management system is implemented through 0.18-micron CMOS process. Based on this topology and technology, low threshold-voltage of MOSFETs is used instead of diodes in order to reduce the power losses of the integrated rectifier circuit. Besides, a single switch with the duty-cycle control is introduced to reduce the complexities of the integrated boost converter. Measurement results show that the realistic performances of the rectifier circuit could be considerably improved based on the performances showed by the existing study.



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## 1. INTRODUCTION

Energy efficiency is having an existed issue in wireless applications. One such solution is energy harvesting technology, which can extract maximum power from the energy harvester. Several researchers have reported a few different energy harvesting mechanisms such as light, thermal, vibration, radio frequency (RF) and so on [1-2]. However, the micro-harvesting systems requires an efficient rectifiers which compact in size to produce as high output power as possible [3].

Due to the compactness of the rectifiers, CMOS technologies are the popular solution to reduce the rectifier circuit size, i.e. 0.5 µm, 0.35 µm, 0.25 µm, 0.18 µm and etc. [4-6]. The most common setup is based on the use of CMOS bridge rectifier as it ensures a full rectification in the simplest way.

The main issue that comes with such CMOS bridge rectifier is related to the MOS devices which are used as switches in the system; accompanied by voltage drops that need to be reduced in order to maintain high output voltage [7]. Various techniques have been employed to reduce the voltage drop. The most recent techniques that capable to control the MOS devices are through the use of threshold voltage and the introduction of active components including comparator circuits. However, the threshold voltage that has been employed in the first technique is relatively high and leading to significant power loss during rectification stage, while the second technique increases the number of MOS devices, which thus adding to the voltage drop [8].

Meanwhile, the CMOS bridge rectifier is also expected to be able to boost up the extracted output power from the micro-harvesting generator. Although the latest reported topologies with voltage doubler function can be employed to increase the output power, a large number of external connections is required, which limits the effort to reduce the size of the overall rectifier. The problem is even more significant if other conditioning circuits such as boost converter, buck converter, voltage inverter, or switch controller circuit are introduced to develop the voltage doubler function circuit, as they could increase the number of dies and complexity of the whole topology [9].

The above-mentioned problems constitute the main issues discussed in this paper, where solutions are proposed by introducing a CMOS rectifier with boost-converter and duty-cycle-control circuit topology that offers compactness and high output power, which both is suitable for wireless power devices in general, and for energy harvester systems specifically.

## 2. RESEARCH METHOD

In Figure 1, the CMOS rectifier with boost converter (BRBS) is proposed to improve the previous rectifier with boost converter in [10], by simplifying the operation circuit and reducing its size. There are only six external connections, where two are connected to the input inductor, two to the load, one to the ground, and another one to the duty-cycle control. It is fabricated into the single die instead of the two dies, which was implemented in [10]. The proposed BRBS circuit should be led to a reduction in overall size and improved the lifespan of the converter [11].

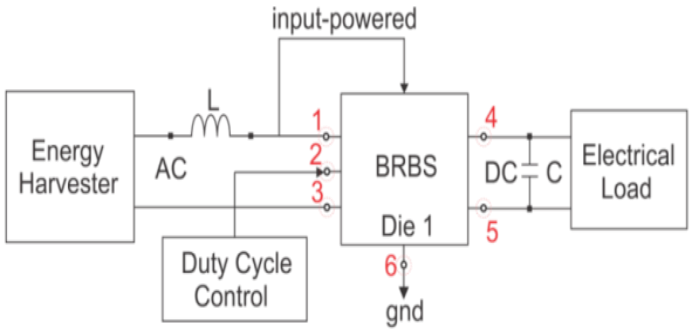


Figure 1. Block diagram of CMOS rectifier with Boost-Converter (BRBS) presents the input-powered converter, which eliminated the pre-charged of the load [11]

The objectives of the proposed CMOS rectifier with boost converter are to (1) reduce the power loss of the rectifier, (2) minimize the complexity of the boost converter, and (3) increase the power conversion efficiency (PCE) in the system. One way to reduce the power loss related with the rectifier is through the diodes removal and replace with the low-threshold-voltage of MOSFETs in the CMOS bridge rectifier. The CMOS bridge rectifier promises the simple and full rectification, whereas the low-threshold-voltage of MOSFETs helps in reducing the voltage drop of the rectifier.

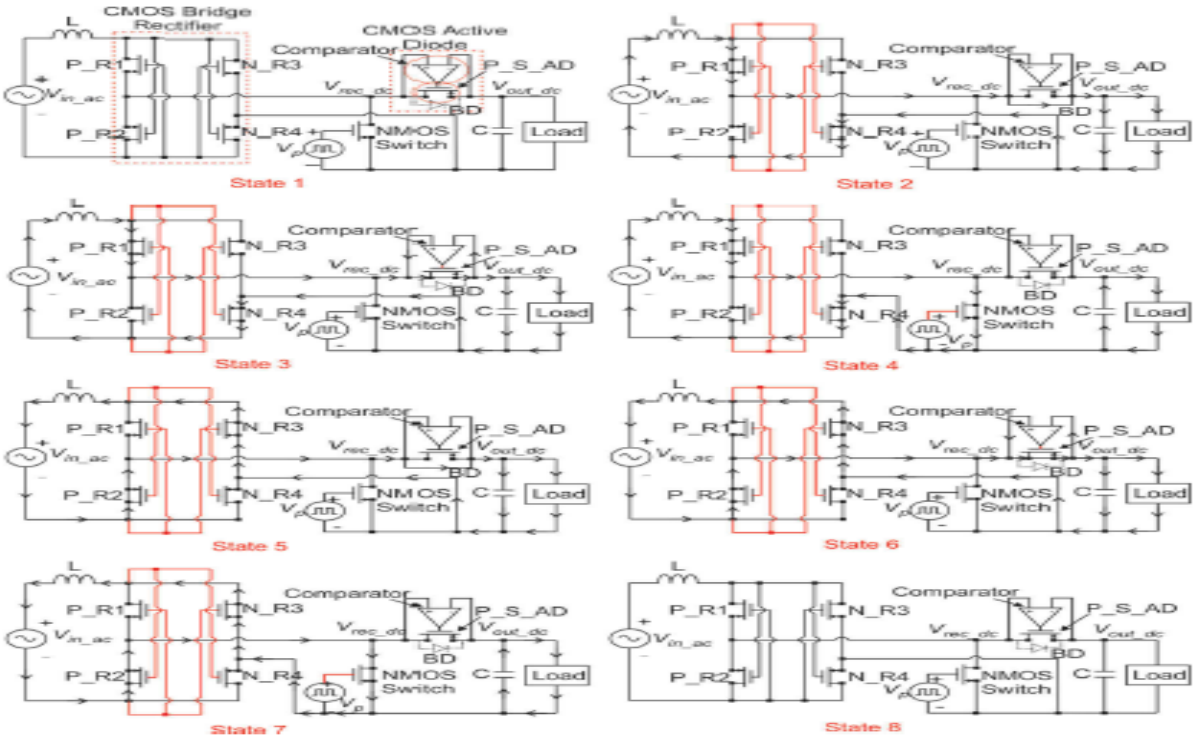


Figure 2. Switching algorithm in proposed CMOS rectifier with boost converter [11]

The boost converter is used in the proposed rectifier because of its easiness in implementing and reducing the number of external connections, which relates to the overall size of the circuit. The boost converter employs two main components, namely NMOS switch and active diode. In Figure 2, NMOS switch works as a boost switch to regulate the dc output higher than the input voltage. When NMOS is turned ON, the energy from the input is stored in the load capacitor; otherwise the energy is released to increase the dc output [11].

Additionally, the active diode in the boost converter employs as a conditional switch to block the reverse current from the load, likewise the load is sustained by the load capacitor. The comparator in active diode is assigned the potential difference between the dc output rectifier and the dc output of the load. When the dc output rectifier is higher than the dc load, the active diode is turned ON, and enables the input energy to be loaded. Otherwise, the active diode is turned OFF to prevent the reverse current flowing back to the input, thus causing power losses.

### 2.1. Mathematical Model of MOSFETs

In order to reduce the voltage drop of the rectifier, the diode-based rectifier is replaced with the low-threshold voltage of MOSFET. In this study, the MOS devices, i.e. NMOS and PMOS are used as the switching devices in the proposed rectifiers as shown in Figure 3. Thus, the characteristics of MOS devices that include the threshold voltage (Vth_MOS) and the gate-source voltage, Vgs are required for observation purposes. Then, the (W/L) size of the MOSFETs is defined by using appropriate mathematical model.

The switching ON and OFF mode of the MOSFETs is depends on the different potential of the gate-source voltage and the threshold voltage. The NMOS would only turn ON when the gate-source voltage is higher than the threshold voltage. Meanwhile, the gate-source voltage which is lower than the threshold voltage is required to turn the PMOS fully ON.

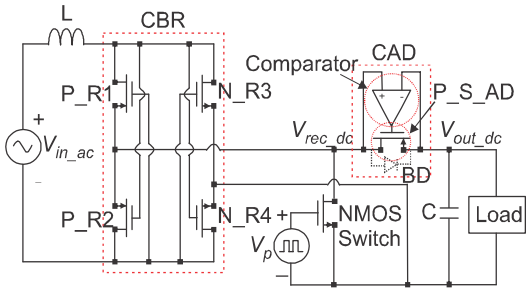


Figure 3. NMOS and PMOS are used as the switching devices in the proposed CMOS Rectifier with Boost-Converter (BRBS) based on 0.18 µm CMOS process technology

The proposed rectifier requires the significant value of W with the constant $KP_N$, in order to achieve feasible $I_d$, thus reduce the leakage current that would lead to the voltage drop. The drain current, Id equation in the saturation region is given as;

$$I_D = \frac{KP_N}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{th\_MOS}\right)^2\left(1+\lambda\left(V_{DS} - V_{DS,SAT}\right)\right) \quad (1)$$

$$I_D = I_{DS,SAT} + \lambda\left(I_{DS,SAT}\right)\left(V_{DS} - V_{DS,SAT}\right) \quad (2)$$

Where, for saturation, $V_{DS} \geq V_{GS\text{-}Vth\_MOS}$ and $V_{GS} \geq V_{th\_MOS.}$ Solving for the drain current using (1) and (2), it becomes.

$$I_D = \frac{KP_N}{2}\left(\frac{W}{L}\right)\underbrace{\left(V_{GS} - V_{th\_MOS}\right)^2}_{V_{DS,SAT}} \quad (3)$$

Where $KP_N$ is defined as the transconductance parameter for a MOSFET. For NMOS, this parameter is stated by:

$$KP_N = \mu_n.C'_{ox} = \mu_n.\frac{\varepsilon_{ox}}{t_{ox}} \quad (4)$$

And for PMOS, it is stated by

$$KP_p = \mu_p.C'_{ox} = \mu_p.\frac{\varepsilon_{ox}}{t_{ox}} \quad (5)$$

Where $\mu n$ and $\mu p$ are the surface electron mobility of the MOSFETs. Meanwhile, Cox is the oxide capacitance per unit area.

Meanwhile, from (3), the size of MOSFET, $S_{N\_R}$ in the proposed rectifier can be calculated as;

$$S_{N\_R} = \frac{W}{L} = \frac{2I_D}{KP_N\left(V_{GS} - V_{th\_MOS}\right)^2} \quad (6)$$

Where $I_d$ is set reasonably high to increase the output power for the low input voltage, where $P \propto I$, thus an assumption has to be made on the $I_d$.

As mention earlier the low-threshold voltage of MOSFETs in the proposed rectifier can be reduce the voltage drop, $V_{ds(sat)}$ by MOSFET, which will be explained as follow;

$$V_{ds,sat} = I_{ds,sat} \times R_{ds(ON)} \quad (7)$$

Let solve the turn-on resistance, $R_{ds(ON)}$ by assuming the drain-source current, $I_{ds,\ sat}$ as equivalent to the drain current, $I_d$ in (3). Meanwhile, the drain-source voltage of MOSFET is equal to the different potential of the gate-source and the threshold voltages $(V_{ds,sat}=V_{GS}-V_{th\_MOS})$.

$$R_{ds(ON)} = \frac{V_{ds,sat}}{I_{ds,sat}}$$
$$R_{ds(ON)} = \frac{\left(V_{GS} - V_{th\_MOS}\right)}{\frac{KP_N}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{th\_MOS}\right)^2} \quad (8)$$
$$R_{ds(ON)} = \frac{2L}{KP_N \times W \times \left(V_{GS} - V_{th\_MOS}\right)}$$

By substitute (8) into (7), the voltage drop of MOSFET is derived as

$$V_{drop} = V_{ds,sat} = \frac{2L \times I_{ds,sat}}{KP_N \times W \times \left(V_{GS} - V_{th\_MOS}\right)} \quad (9)$$

From (9), the size of MOSFET should be designed properly to reduce the voltage drop and thus, increase the output power.

## 3. RESULTS AND ANALYSIS

Simulation results by using Cadence simulation tool were presented in order to verify the effects of the W/L size of MOSFET on the voltage drop for the proposed rectifier. Based on equation (9), the W/L size of MOSFET was observed as the important parameter when associated with the reduction of the voltage drop. The size of NMOS and PMOS in the CMOS rectifier (CBR) must be symmetrical, in order to monitor the current flow of the circuit.

Figure 4 shows the simulated output voltage with the voltage drop when the different sizes of MOSFETs (see Table 1) were used in the proposed rectifier. It shows that the smaller W/L ratio (50/0.18, 250/0.18 and 500/0.18) dropped the output voltages from 1% to 5%. In this case, the smaller MOSFETs are not enough to reduce the turn-on resistance, which then contributed to the higher voltage drop and power consumption of rectifier. On the other hand, the larger MOSFETs is purposely neglected in order to avoid the leakage current and large area of the active circuit. Therefore, the W/L size of 750/0.18 in micron-meter is chosen for all the MOSFETs in the CMOS rectifier.

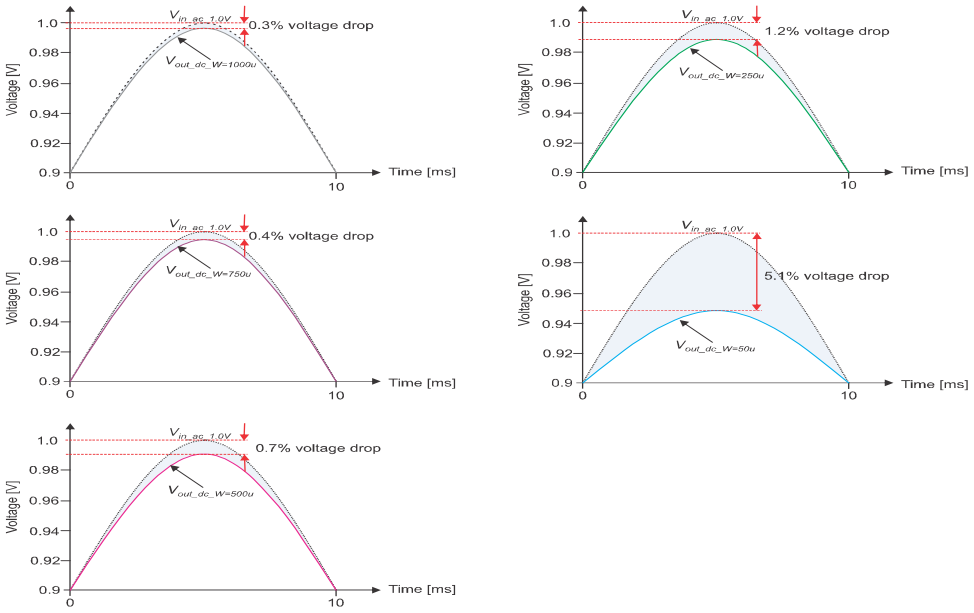


Figure 4. Simulated output voltage with the voltage drop for different size of MOSFETs in the proposed rectifier. Vin=1.0 Vac, $f$in=50 Hz and Rload=2 kΩ

Table 1. The Simulated Output Voltage with the Voltage Drop for Different Size of MOSFETs in the Proposed Rectifier

| W/L ratio | Vout (V) | Vdrop (%) $= \frac{Vdrop}{(Vin - Vout) * 100}{Vin}$ |
|---|---|---|
| 50/0.18 | 0.949 | 5.1 |
| 250/0.18 | 0.988 | 1.2 |
| 500/0.18 | 0.993 | 0.7 |
| 750/0.18 | 0.996 | 0.4 |
| 1000/0.18 | 0.997 | 0.3 |

Figure 5 illustrates the simulation results of the output voltage and output power at the different duty-cycle (see Table 2). The duty-cycle is varied from 10% to 90% based on the previous reported works. The objective of the used the duty-cycle control is to achieve output voltage regulation, thus reducing the switching losses. The choice of duty-cycle is obtained with the assumption of the switching frequency, $fs$ is much higher than the line frequency, $fin$.

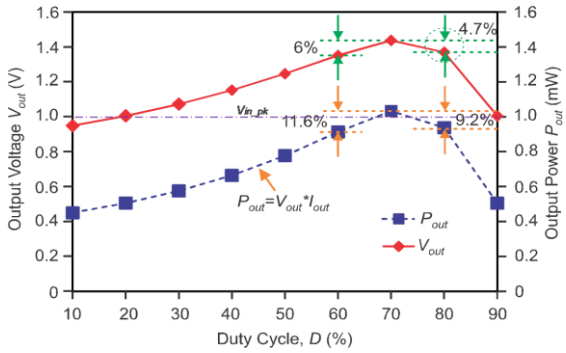


Figure 5. Simulated output voltage and output power with variation of duty cycle

Table 2. The Simulated Output Voltage and Output Power with Variation of Duty Cycle

| Duty Cycle, D (%) | Vout (V) | Pout (mW) (5) |
|---|---|---|
| 10 | 0.948 | 0.45 |
| 20 | 1.005 | 0.50 |
| 30 | 1.072 | 0.58 |
| 40 | 1.152 | 0.66 |
| 50 | 1.246 | 0.78 |
| 60 | 1.351 | 0.91 |
| 70 | 1.437 | 1.03 |
| 80 | 1.369 | 0.94 |
| 90 | 1.004 | 0.50 |

A result shows that there is a relationship between the duty-cycle and the output voltage, where the output voltage was increased when the duty-cycle is increased. However, the output voltages are dropped when the duty-cycle is higher than 70%. It can be seen that a duty-cycle at 70% as an optimization value to obtain the higher output voltage, since the high output regulation is required in this design.

The design of the CMOS Rectifier with Boost-Converter (BRBS) is carried out using a SilTerra 0.18 µm CMOS technology. The dimension of the active area is 24 nm2 (93 µm × 255 µm) as shown in Figure 6, which is 80% to 83% smaller than the previous reported works [10], [12].

The measurement setup is shown in Figure 7, where the complete interface circuits such off-chip voltage sources and electrical components including input inductance, load resistance, and capacitance are arranged on the breadboard. The parameters and the testing conditions which implemented in the measurement are listed in Table 3.

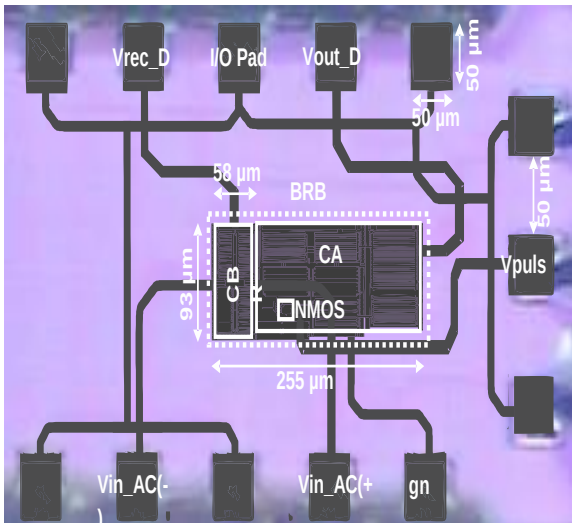


Figure 6. Photomicrograph of the fabricated rectifier (BRBS) in 0.18 µm CMOS technology

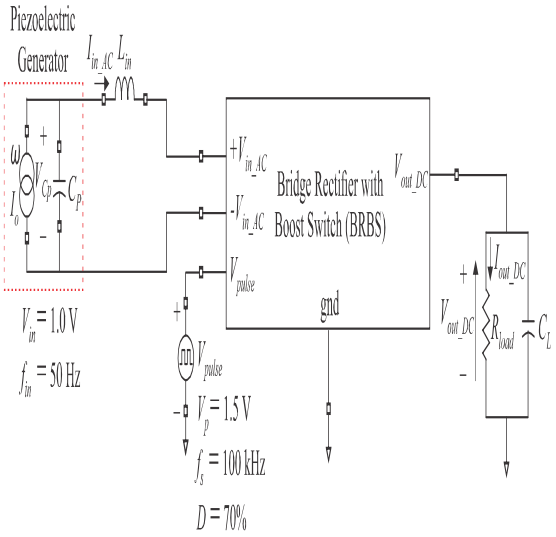


Figure 7. Measurement setup

Table 3. List of Parameters and Testing Conditions

| Parameters | Implementations |
|---|---|
| Input voltage amplitude, $V_{in}$ | 1.0 V |
| Input Frequency, $f_{in}$ | 50 Hz |
| Switching Frequency, $f_s$ | 100 kHz |
| Duty Cycle, $D$ | 70% |
| $R_{load}$ | 2 kΩ |
| $L_{in}$ | 1 mH |
| $C_{load}$ | 100 µF |

Measurements were carried out to evaluate the performance of the proposed CMOS rectifiers. Figure 8 shows the measured output voltages for the both rectifiers; CBR and BRBS with the reference input voltage. Here, the output voltage of the BRBS circuit achieves 21% higher than the reference input voltage. Compared to the CBR circuit, the BRBS circuit achieves a higher output voltage due to voltage doubler function in boost converter. Moreover, the BRBS circuit obtains a considerably higher output power during the comparison with other design listed in Table 4.

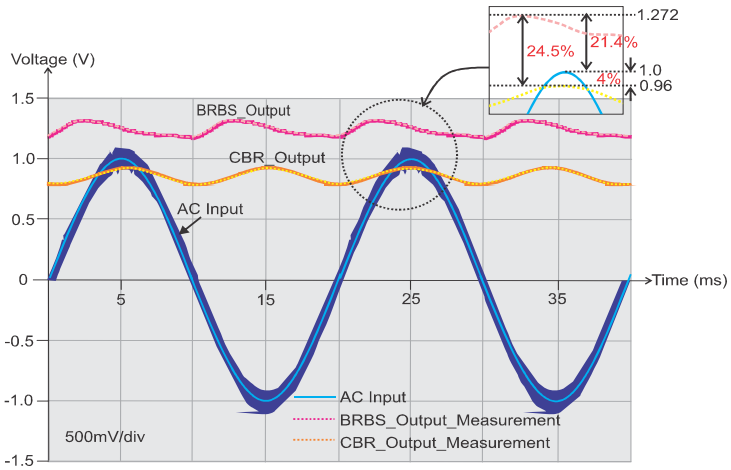


Figure 8. Measured output voltages of the proposed CMOS Rectifier without Boost-Converter (CBR) and CMOS Rectifier with Boost-Converter (BRBS) circuits

Table 4. Comparison between the Rectifiers with Voltage Doubler Function in Energy Harvesting Applications

| Previous Work | [10] | [12] | This Work |
|---|---|---|---|
| Technology | 0.5 µm CMOS | 0.35 µm CMOS | 0.18 µm CMOS |
| Topology | Input-Powered AC/DC Converter | Dual-output AC/DC Rectifier | CMOS Rectifier with Boost-Converter (BRBS) circuit |
| Switch Control Technique | Boost Converter | Voltage Doubler | Boost Switch |
| $P_{out}$ (W) | 3.9 m ($I_{load}$=1.3 mA) | 0.5 m | 1.65 m ($I_{load}$=1.3 mA) |
| $V_o/\|V_{in}\|$ | 3.0/1.5 | N/A | 1.272/1.0 |
| $f_{in}$ (Hz) | 20 | 200 | 50 |
| ` | 0.143 (2 Dies) | 0.133 | 0.025 (1 Die) |

## 4. CONCLUSION

An enhanced high output power and compact CMOS rectifier with boost-converter and duty-cycle-control circuit has been presented. This topology of integrated rectifier solves the energy efficiency issue associated with the voltage drop of MOS devices and low output power of micro-harvesting generator. A CMOS bridge rectifier with boost converter is implemented which uses the low-threshold voltage of MOSFETs in order to reduce the rectifier voltage drop. Meanwhile, a boost converter with a duty-cycle control is used to achieve output voltage regulation, thus reducing the switching losses and enhancing the efficiency of an overall circuit.

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